DL405

Slice I/O Master & Slave

Manual Number D4-SLICE-M

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Manual Revisions

If you contact us in reference to this manual, be sure to include the revision number.

Title: DL405 Slice Master/Slice Slaves
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Issue	Date	Effective Pages	Description of Changes
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Table of Contents

Chapter 1: Getting Started

Chapter 2: Designing the Slice I/O System

Chapter 3: Installation & Wiring

Chapter 4: Writing the Setup Program

1

Getting Started

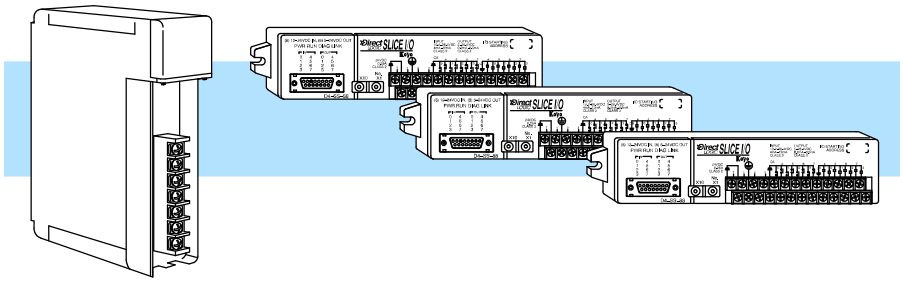
In This Chapter. . . .

- Introduction
- Manual Layout
- What is Slice I/O
- Slice Master (D4-SM) Features
- Slice Slave (D4-SS-xx) Features
- Addressing Modes
- Assigning the Remote Input and Output Addresses
- How the CPU Updates Slice I/O Points
- 3 Easy Steps for Setting Up Slice I/O

Introduction

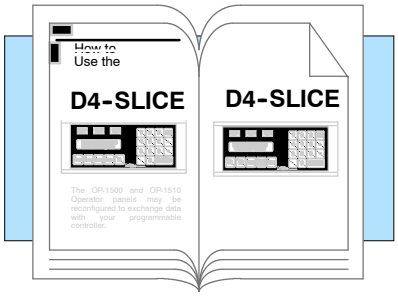
The Purpose of this Manual

This manual shows you how to install, program, and maintain the DL405 Slice I/O system. It also helps you understand the system operation characteristics. .



Contents of the Manual

If you understand PLC systems, this manuals will provide all the information you need to get and keep your Slice I/O system up and running. We will use examples and explanations to clarify our meaning and perhaps help you brush up on specific features used in the DL405 system. This manual is not intended to be a generic PLC training manual, but rather a user reference manual for the DL405 Slice I/O system



Supplemental Manuals

Depending on the products you have purchased, there may be other manuals necessary for your application. You will want to supplement this manual with any other manuals written for other products. We suggest:

- D4-USER-M (the DL405 User Manual)
- DA-DSOFT-M (the ***Direct***SOFT User Manual, which is included with the ***Direct***SOFT Programming software)

Where to Begin

If you are in a hurry and already understand the basics of remote I/O systems,you may only want to skim this chapter, and move on to Chapter 2, Installation and Wiring. Be sure to keep this manual handy for reference when you run into questions. If you are a new DL405 customer, we suggest you read this manual completely so you can fully understand the Slice modules, configurations, and procedures used. We believe you will be pleasantly surprised with how much you can accomplish with PLC***Direct***™ products.

If you're really in a hurry, check the diagram shown on Pages 1-14 and 1-15. It shows how the system design, hardware settings, programming, and memory map tables are used to develop a working system.

Technical Assistance

After completely reading this manual, if you are not successful with implementing the OP-1500 or OP-1510, you may call PLC***Direct*** at (800) 633-0405, Monday through Friday from 9:00 A.M. to 6:00 P.M. Eastern Standard Time. Our technical support group will work with you in answering your application questions. If you have a comment or question about our products, services, or manuals which we provide, please fill out and return the suggestions card included with this manual.

Chapters The main contents of this manual are organized into the following four chapters.

1	**Getting Started**	contains basic information you need to know in order to get started. It includes a brief description of a Slice I/O system, an explanation of who needs such a system, and an overview of the basic system components and the steps necessary to develop a working system.
2	**Designing the Slice I/O System**	shows the steps required to design your system. It includes a tutorial on how to use worksheets to keep track of all the I/O address assignments. It provides the framework for developing the necessary information you will need for programming and hardware setup.
3	**Installation and Communication Wiring Guidelines**	shows you how to install the Slice Master and Slice Slave units. This chapter includes wiring information, shows you how to set the rotary dial and dip switch on each module, how to daisy chain the remote units, how to size and use termination resistors, and how to connect the Run Output circuit.
4	**Writing the Setup Program**	shows you how to use ***Direct***SOFT to write the Slice I/O setup program. This chapter takes the information developed from your worksheets and helps you develop a working program. This includes showing you how to map certain addresses together in order for the I/O status of each Slice I/O unit to be read and written to the CPU's memory image area. You will also be shown how to use certain internal relays to monitor communications status, build error traps, and perform other useful functions.

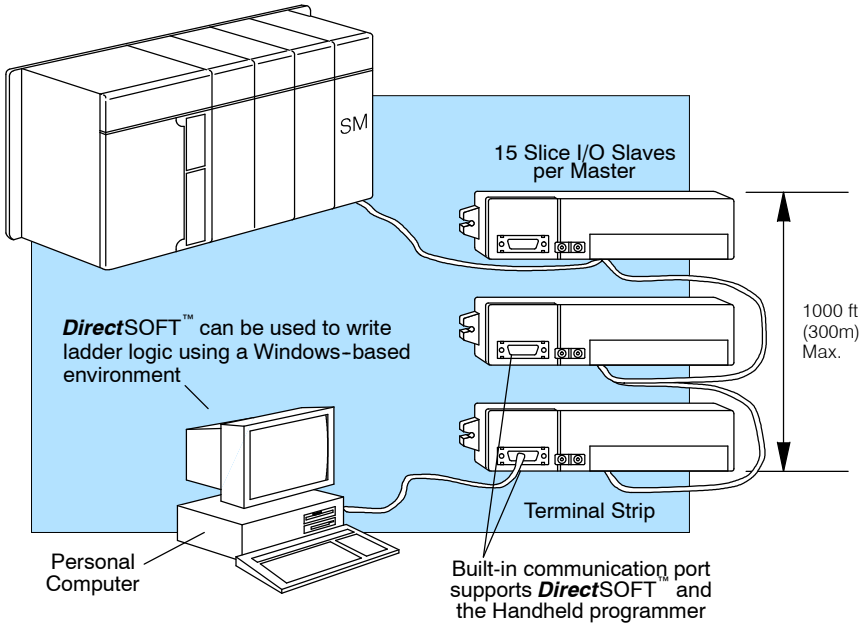
Appendices Additional examples and reference information are in the following three appendices:

A	**Writing the Setup Program**	includes a blank worksheet that can be copied and used for designing your system.
B	**Memory Tables for Remote I/O Addresses**	shows the reserved memory locations for the transfer of Slice I/O data. It is cross-referenced by data type.
C	**Determining I/O Update Time**	shows you how to calculate the amount of delay inherent with the transfer of data back and forth between the master and its Slice slaves. Provides tables for all four baud rates available, based on number of I/O points used.

What is Slice I/O?

A Slice I/O system is simply another cost-effective form of remote I/O which allows you to locate I/O modules at remote distances from the CPU base, without using separate I/O bases. These remote units have no CPU of their own, and are completely controlled by the CPU in the main base via a special module called a **Slice Master**. Each **Slice Slave** (consisting of an internal power supply and I/O adapter circuitry) exchanges data with the CPU in the main base via the master module. The communications link between the master and its slaves is provided by twisted-pair cable. Up to 512 remote I/O points can be supported by either the DL430 or DL440 CPU's, with baud rates of 19.2K, 38.4K, 153.6K and 614.4K.

Example Slice I/O with one master and three slaves



When Do You Need Slice I/O?

Slice I/O offers tremendous savings on wiring materials and labor costs for systems with field devices that are in clusters at various spread-out locations. With the CPU in a main control cabinet or some other central area, only the Slice I/O communications cable is brought back to the CPU base. This avoids the use of a large number of individual field wires over greatly separated distances to all the various field devices. By locating the Slice I/O modules close to the field devices, wiring costs are reduced significantly.

Each slave has a built-in communications port which supports connection to a computer or handheld programmer. This permits system programming from a remote location.

Another inherent advantage of Slice I/O is the ability to add Slice slave units, or temporarily take a unit off line, without disrupting the operation of the remaining system.

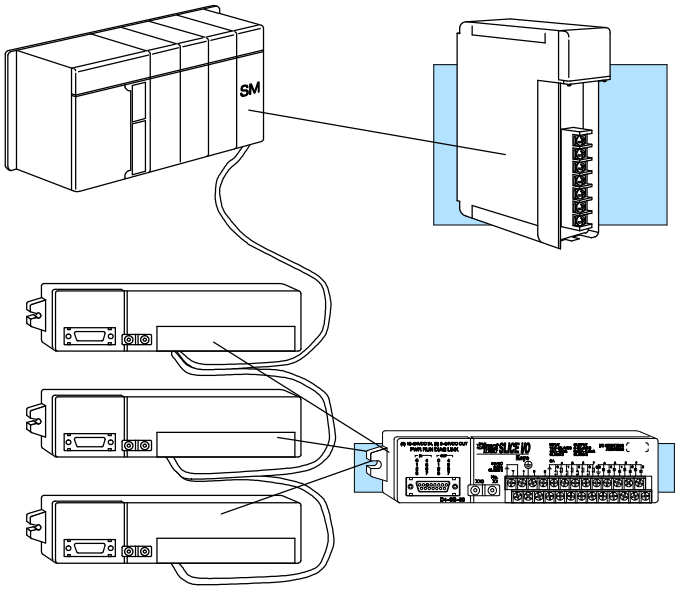
How Does Slice I/O Compare to Standard Remote?

Compared to standard remote I/O systems (e.g. D4-RM and D4-RS combinations), the Slice I/O system is more economical and can support more slaves per channel. It cannot, however, have as much distance between the master and slaves as the conventional remote I/O system. The furthest distance from the master that a slave can be located for the Slice system is 1000 feet. For the conventional remote system, the furthest distance that a slave can be located from its master is 3300 feet. You must examine the needs of your application to determine which type of remote I/O system is best for you.

How Does the DL405 Support Slice I/O?

With the DL405 system, up to 512 remote I/O points can be supported by the DL440 CPU or the DL430 CPU.

The Slice Master is placed in the CPU base. The Master (D4–SM) controls up to 15 Slice Slaves (D4–SS–88, D4–SS–16T, D4–SS–16N, and D4–SS–106).



Slice Master -The D4-SM can link up to 15 Slice slaves (using discrete addressing) per master module. It is mounted in the CPU base. Up to 2 masters can be used.

Note: *There are three different addressing modes available for assigning I/O points to the system. The number of slaves that can be used will vary depending on the method used. This is discussed in detail later.*

Slice Slave - The Slaves are linked together in a daisy chain fashion and are connected to the Master with a twisted pair cable. Each slave must be powered externally by 24 VDC. If you plan to connect a handheld programmer or some other operater interface requiring power from the RS232 port on the front of the unit, then you will have to make sure your power supply has the proper current rating. Slaves require 60mA (max) at 24 VDC without a handheld programmer, but require 250mA (max) with a handheld programmer. At time of publication, Slice Slaves are available as follows:

D4-SS-88 (8 inputs, 8 outputs)
D4-SS-106 (10 inputs, 6 outputs)
D4-SS-16N (16 inputs)
D4-SS-16T (16 outputs)

Number of Masters and Slaves Allowed

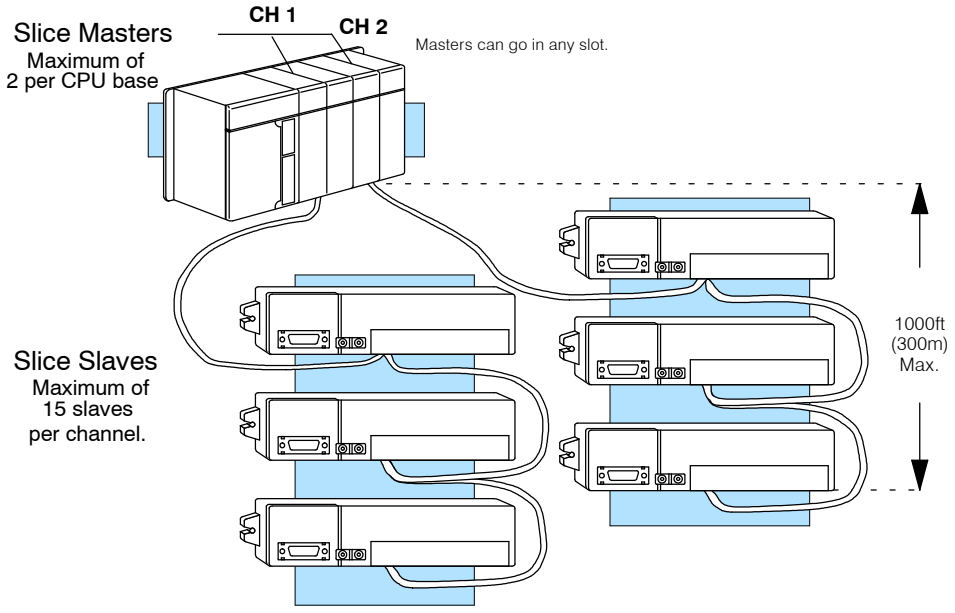
In a simple application, you may want to use only one master in your CPU base and then attach from 1 to 15 Slice I/O units. However, in addition to this basic configuration, more than one master can be placed in the CPU base. You may use a maximum of two masters per CPU base.

The actual number of Slice I/O units that can be connected depends on the addressing mode selected. The various modes are discussed in more detail later.

- **Automatic Addressing** — 12 slaves. In a system with two masters, you can only have one master using automatic addressing. The other master is subject to the following limits.
- **Manual Addressing** — 15 slaves per master
- **Discrete Addressing** — 7 slaves per master

Here is an example where we have placed two masters in the CPU base and then attached a total of six Slice I/O units.

Two Masters in the Same Base (2-Channel)



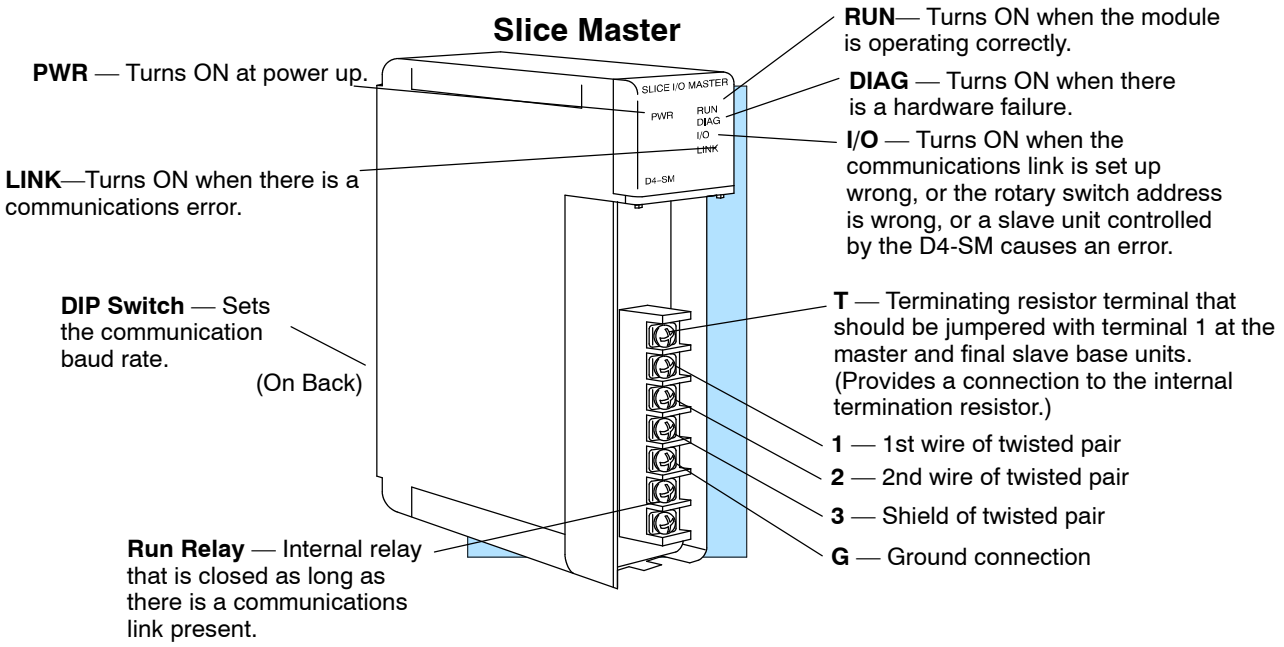
Allowable distance is from furthest slave to the Slice master.

Distance Between Slaves and Master, Baud Rates

Each slave belonging to the same master is hooked together in a daisy chain using a shielded twisted pair cable. The last slave unit in the daisy chain cannot be further than 1000 feet from the CPU base. Each has an address and should be numbered sequentially from 1 through 15 (decimal). You assign this address by setting rotary switches on the front of each slave unit. There are additional switches on the back of each unit to set the communication baud rate. You have your choice of 19.2, 38.4, 153.6, and 614.4 Kb/s. All Slaves and the Master must be set to the same baud rate.

Let's now take a closer look at the Master module and the Slaves.

Slice Master Features (D4-SM)



Specifications

Number of Masters per CPU	2 max. for DL430 or DL440
Maximum No. Slaves Supported	15 per master (total 30 per 2-master system)
Number of Remote I/O Points per CPU	512
Module Type	Intelligent
Installation Requirements	Any slot, CPU base only
Internal Power Consumption	300 mA maximum
Digital I/O Consumed	None
Run Output Relay Rating	250 VAC at 1A 30 VDC at 1A
Communication Baud Rates	19.2, 38.4, 153.6, 614.4 kB (Switch Selectable)
Communication Method	Asynchronous (half-duplex)
Communication Cabling	RS-485 twisted pair Belden 9271 or equivalent
Maximum Transmission Distance	1000 ft. (approx. 300 meters)
Operating Temperature	32 to 140° F (0 to 60° C)
Storage Temperature	-4 to 158° F (-20 to 70° C)
Relative Humidity	5 to 95% (non-condensing)
Environmental air	No corrosive gases permitted
Vibration	MIL STD 810C 514.2
Shock	MIL STD 810C 516.2
Noise Immunity	NEMA ICS3-304 (1500 V 1 minute)

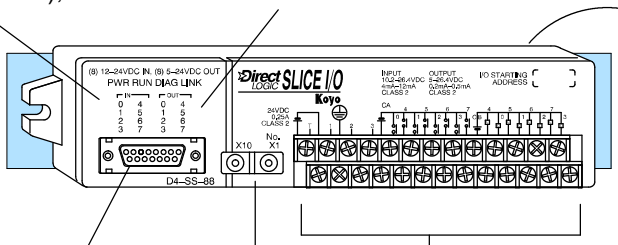
Slice Slave Features (D4-SS-xx)

The following Slice slave units are available:

- D4-SS-88 — 8, 12-24VDC Inputs; 8, 5–24VDC Outputs
- D4-SS-106 — 10, 12-24VDC Inputs; 6, 5–24VDC Outputs
- D4-SS-16T — 16, 5–24VDC Outputs
- D4-SS-16N — 16, 12-24VDC Inputs

Input LED's—These correspond to the numeral indicated plus the starting base address, i.e. (X200+1), (X200+2), etc.

Output LED's—These correspond to the numeral indicated plus the starting base address, i.e. (Y200+1),(Y200+2), etc.



DIP Switch—Used to set the baud rate for communication with the master module. Located on the back of the unit.

Com Port—15 pin female D-shell communications port. This port is identical to the top port on the DL405 CPUs. You can program or monitor the CPU with a handheld programmer or ***Direct***SOFT through this port. You can also connect a DV-1000 Operator Interface to this port.

Connection Screws—For attaching power supply, twisted pair communication cable, and input and output points. Varies by model number.

Rotary Switches—Used to set unit address.

General Specifications

Slaves per channel (See text for details)	15, 12 or 7 depending on addressing mode
Module Type	Non-intelligent slave
Installation Requirements	No base required
Power Required	24 VDC (external) +/- 15% 60mA max. at 24 VDC with no handheld programmer 250mA. max at 24 VDC with a handheld programmer
Run Output Relay Rating	250 VAC at 1A 30 VDC at 1A
Communication Baud Rates	19.2, 38.4, 153.6, 614.4 kB (Switch Selectable)
Communication Cabling	RS-485 twisted pair Belden 9271 or equivalent
Operating Temperature	32 to 140° F (0 to 60° C)
Storage Temperature	-4 to 158° F (-20 to 70° C)
Relative Humidity	5 to 95% (non-condensing)
Environmental air	No corrosive gases permitted
Vibration	MIL STD 810C 514.2
Shock	MIL STD 810C 516.2
Noise Immunity	NEMA ICS3-304

Slice Slave Input Specifications

Rated Input Voltage	12-24 VDC
Operating Voltage	10.2-26.4 VDC
Input Current	3.8 mA @ 12 VDC 8.3 mA @ 24 VDC
Maximum Voltage	26.4 VDC
ON Current/Voltage	>3.5 mA @ 10.2 VDC
OFF Current/Voltage	<1.5 mA @ 4.0 VDC
OFF to ON Response	<7 ms
ON to OFF Response	<12 ms
Number of input points	D4-SS-88: 8 (Consumes 16 inputs, however) D4-SS-16N: 16 D4-SS-16T: None D4-SS-106: 10 (Consumes 16 inputs, however)
Commons	D4-SS-88: 8 points per common D4-SS-16N: 16 points per common D4-SS-16T: N/A (no input available) D4-SS-106: 10 points per common
Wire Gauge	AWG22-AWG18

Slice Slave Output Specifications

Output Circuitry	NPN Open Collector
Operating Voltage	4.5-26.4 VDC
Output Current	0.5A / point (subject to derating, see Chapter 3) 3.0A / common
Maximum Voltage	40 VDC
Maximum Leakage Current	0.1mA @ 40 VDC
ON Voltage Drop	1.0V @ 0.5A
Smallest Recommended Load	0.2mA
Maximum Inrush Current	1.0A for 100ms 2.0A for 10ms
OFF to ON Response	0.5ms
ON to OFF Response	0.5ms
Fuses	1, 5.0A fuse per output common
Number of output points	D4-SS-88: 8 (Consumes 16 outputs, however) D4-SS-16N: None D4-SS-16T: 16 D4-SS-106: 6 (Consumes 16 outputs, however)
Commons	D4-SS-88: 1, 8 points per common D4-SS-16N: N/A (no outputs available) D4-SS-16T: 2, 8 points per common D4-SS-106: 1, 6 points per common
Wire Gauge	AWG22-AWG18

Addressing Modes

What is Addressing?

In order for the CPU to recognize the I/O points in a Slice I/O system, the I/O must first be configured by writing setup information to special V-memory locations. This configuration process is called “addressing”. The addressing process links (also referred to as “maps”) the I/O data stored in the Slice master module with the memory of the PLC. We’ll show you more about this addressing process in a moment.

3 Modes of Addressing Available

Later in this manual, you will learn how to use any of three possible modes to assign slice I/O addresses:

- **Automatic:** With this mode, your CPU will automatically assign your Slice *inputs* and Slice *outputs* starting with X200 and Y200 respectively. This means the X200/Y200 I/O points cannot already be assigned to some other module; otherwise, there would be an address conflict. This mode also consumes at least 16 input points and 16 output points per slave, even if the slave does not have 16 points. This means the addresses associated with the Slice I/O inputs start at X200 and extend to *at least X220*, and for the outputs, start at Y200 extending to *at least Y220*. Even if you don’t use all of these I/O points, they are consumed by the system and you cannot have unused I/O assigned to local I/O.

NOTE: There is a limit to how many slaves you can use with a master that has been configured automatically. You can only attach a maximum of 12 slaves to a master that has been configured automatically. Additionally, if you use a second master, only one of the masters can be addressed automatically.

- **Manual:** With this mode, you must select data types. You have your choice of using X Y, C or GX data types. These data types will be explained in more detail a little later. Manual addressing can be used with one or two masters. *Manual addressing allows a maximum of 15 slaves per master.*

  Unlike automatic addressing, you choose the starting addresses for the manual mode. There are tables in Appendix B to help you do this. Everything is assigned in blocks of 16 bits; so you can’t just use 8 consecutive bits for your Slice I/O assignment and assign the other 8 bits for local I/O. You are committed to 32 points for each slave (16 inputs, 16 outputs).
- **Discrete:** This is very similar to manual addressing with two exceptions: **(1)** You are not committed to 16 inputs and 16 outputs in some cases. For example, if you discretely addressed a D4-SS-106 slave, the 32-point comsumption rule says that even you will consume 16 input points and 16 output points, even though you are only actually using 10 inputs and 6 outputs. But take another example where you are discretely addressing either the D4-SS-16N or the D4-SS-16T. Each of these would only consume 16 points per slave. (This is discussed in more detail in Chapter 2.)
  (2) *Discrete addressing allows a maximum of 7 slaves per master.* Discrete addressing, like manual addressing, requires that you choose data types among the X, Y, C and GX options. Again, this will be discussed in detail later.

Assigning the Remote Input and Output Addresses

Automatic Addressing for Local and Expansion I/O

If you've used a DL405 CPU and local (or expansion) I/O before, then you probably know that the CPU will automatically assign the input and output addresses for local or expansion I/O. That is, input points are automatically assigned starting at X0, and output points are automatically assigned starting at Y0.

The Affect of Automatic Addressing on Slice I/O

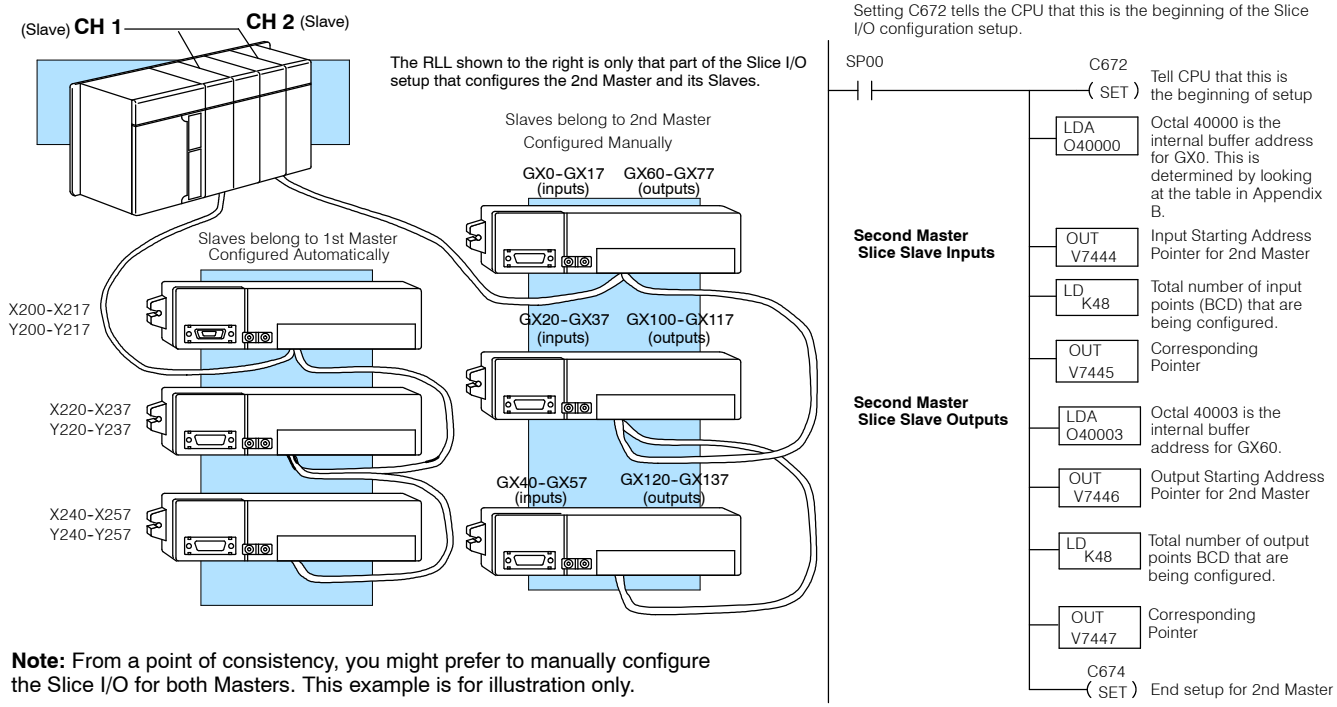
A Slice I/O system uses the automatic addressing concept, but it *is not* related to the automatic configuration that is done by the CPU for the local and expansion I/O. The local and expansion addressing will start at X0 and Y0 for inputs and outputs. The Slice I/O automatic addressing starts at X200 and Y200 for input and output points. There are three key things to remember with the Slice I/O and automatic addressing.

- If your local and/or expansion I/O uses input and/or output points above X200 or Y200, then you can't use automatic addressing for the Slice I/O.
- You can only use automatic addressing for one master in a Slice I/O system. With two masters, one must use discrete or manual addressing.
- The CPU will assign X's starting at X200 and assign Y's starting at Y200, at the rate of 16 input and 16 output points per slave unit.

Manual or Discrete Addressing for those Points Not Automatically Configured

For manual or discrete addressing, the DL405 CPUs have specific memory locations (called pointers) that tell the CPU how to assign the Slice I/O addresses . The starting address for the pointers of the 1st Slice Master starts with V7404 and the starting address for the pointers of the 2nd Slice Master is V7444. Your RLL must store addresses in these pointer locations to tell the CPU where the Slice I/O will appear in the I/O image area. In the example below, the CPU will automatically configure the I/O of the 1st Slice Master and use global (GX) I/O points to manually configure the 2nd Slice Master. Don't worry about understanding everything shown below. Chapter 4 will provide the missing details.

Example Slice I/O Address Assignment



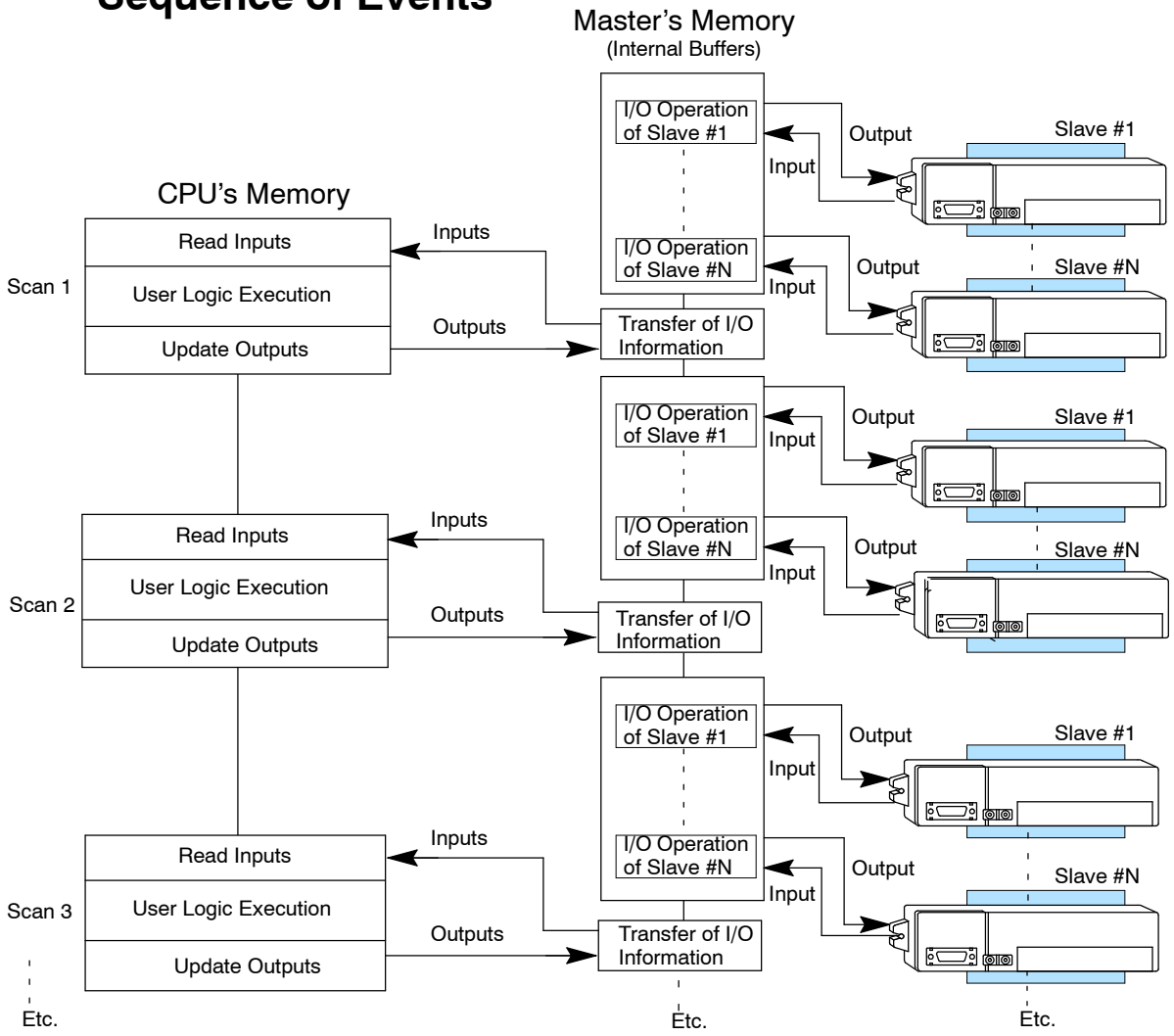
Note: From a point of consistency, you might prefer to manually configure the Slice I/O for both Masters. This example is for illustration only.

How the CPU Updates Slice I/O Points

The CPU and Slice Master work together to update the remote Slice I/O points. Below is an example showing how scanning and updating takes place. Notice that there are two independent scan cycles going on at the same time, but asynchronously. The CPU module is doing its scan which includes looking at the information that the master is writing to its internal buffers.

During every CPU scan, the CPU examines the internal buffers of the Slice Master, and updates input and output data from the Slice I/O. It is very possible for the CPU to be scanning faster than the Slice Master can do its scan. It is largely dependent on the size of the application program, the baud rate you have selected for the data transfer between the slaves and master, as well as the number of I/O points being monitored.

Sequence of Events

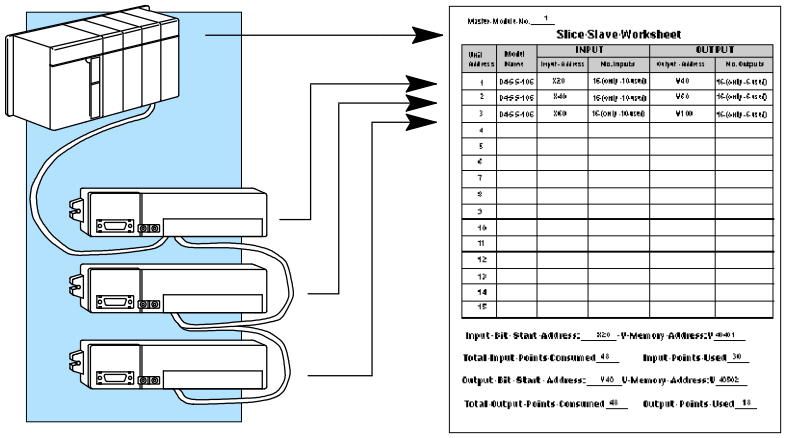


NOTE: In some cases it may be helpful to understand the update time required for a Slice I/O system. Appendix C shows example calculations.

3 Steps for Setting Up Slice I/O

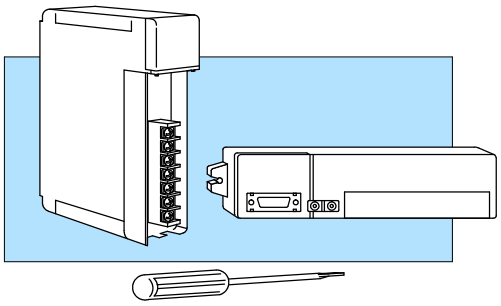
Step One: Design the System

First figure out how many I/O points you will need at each remote drop. This will tell you how many Slice masters and Slice slaves you will need. **In Chapter 2**, we will show you how to use worksheets to plan and keep track of your data type assignments. We'll also show you how to determine the correct addresses for reading and writing the Slice I/O data.



Step Two: Install the Components

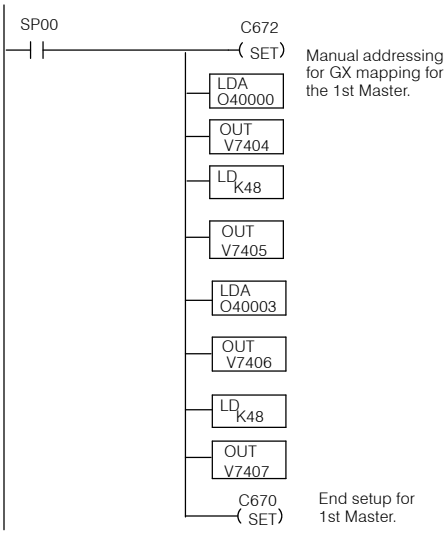
Set the hardware switches so that the CPU can identify the master and slave units. This also will set the baud rate for data transfer and designate how the slave units are numbered, i.e. No. 1, No. 2, and so on. Then, insert the master(s) into the base, and mount the slaves. Wire all of your I/O to match your information in Step 1. **Covered in Chapter 3.**



Step Three: Write the Setup Program

Write the RLL setup program. **Covered in Chapter 4**.

The next two pages provide a complete overview of the entire process for an example Slice I/O system. Of course, to learn all of the details, you should read each chapter carefully.

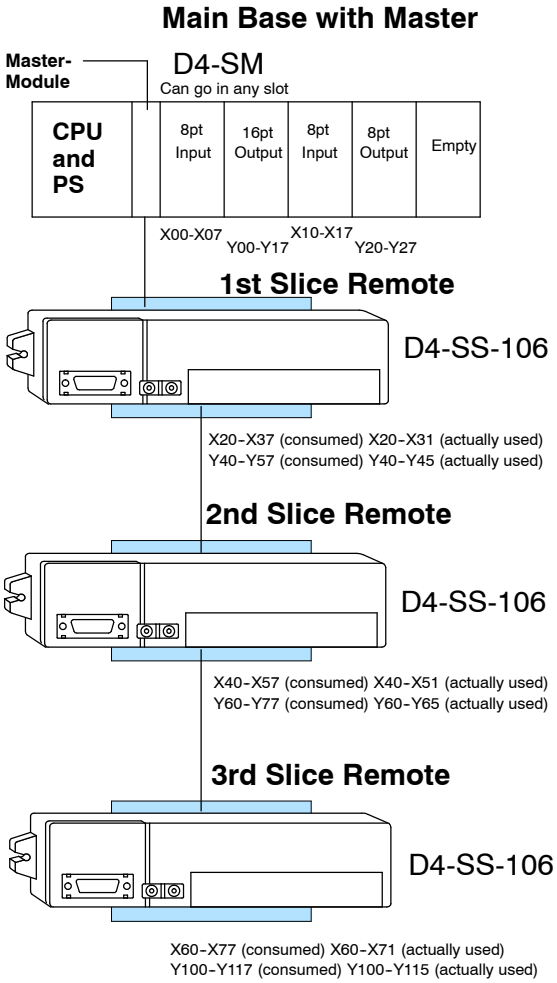


EXAMPLE:

In this example, we are using only one master and three Slice slaves. We are setting the baud rate to 153.6 kB and we are using manual addressing. The address assignments shown for the modules in the local base consume X0–X17 and Y0–Y27. Therefore we are starting our manual addressing for the slaves at X20 and Y40. (We could not start at Y30 because the addresses must start on a 16pt. boundary.)

Step 1: Design the Slice I/O System

The worksheet is included in Appendix A. You don't have to use a worksheet, but it may help organize your planning and even make the task of writing your ladder logic a little easier. You can have up to two masters per system. If you use a second master, you will have to fill out two of these sheets. Even though we could have up to 30 slaves (15 per master) with manual addressing, we have only used three in this simple example. See note below for other types of addressing and the respective limitations on number of slaves supported.



Master Module No. 1

Slice Slave Worksheet

Unit Address	Model Name	INPUT		OUTPUT	
		Input Address	**No. Inputs**	Output Address	**No . Outputs**
1	D4-SS-106	X20	16 (only 10 used)	Y40	16 (only 6 used)
2	D4-SS-106	X40	16 (only 10 used)	Y60	16 (only 6 used)
3	D4-SS-106	X60	16 (only 10 used)	Y100	16 (only 6 used)
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					

Input Bit Start Address: X20 **V-Memory Address:V** 40401

Total Input Points Consumed 48 **Input Points Used** 30

Output Bit Start Address: Y40 **V-Memory Address:V** 40502

Total Output Points Consumed 48 **Output Points Used** 18

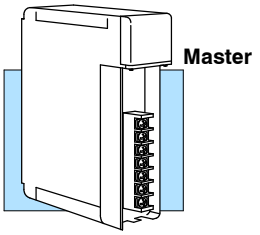
Note: Manual addressing will support 15 slaves per master. Automatic addressing will support 12 slaves per master. Discrete addressing will support 7 slaves per Slice master. Automatic addressing can only be used by one of two masters mounted in the CPU base. Manual and discrete addressing can be used with both masters.

Step 2: Set the Hardware

Table for setting DIP switch

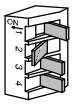
Baud Rate		19.2kB	38.4kB	153.6kB	614.4kB
Master	1	OFF	ON	OFF	ON
	2	OFF	OFF	ON	ON
	3	Not used, should be set to OFF			
	4	See Chapter 3*	See Chapter 3*	See Chapter 3*	See Chapter 3*
Remote	1	OFF	ON	OFF	ON
	2	OFF	OFF	ON	ON

Settings for this Example



Baud Rate for Link

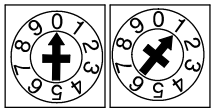
(Master and Slave must match.)



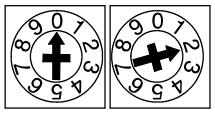
Set to: 153.6 kB

On Back

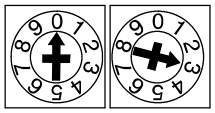
Unit Address



On Front



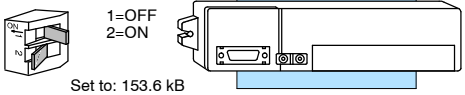
On Front



On Front

Baud Rate for Link

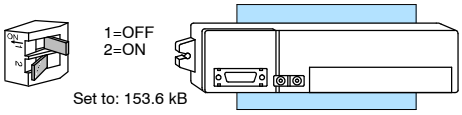
1st Slice Remote



Set to: 153.6 kB

On Back

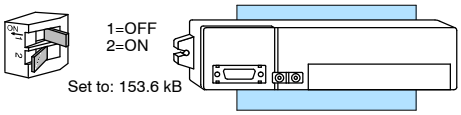
2nd Slice Remote



Set to: 153.6 kB

On Back

3rd Slice Remote



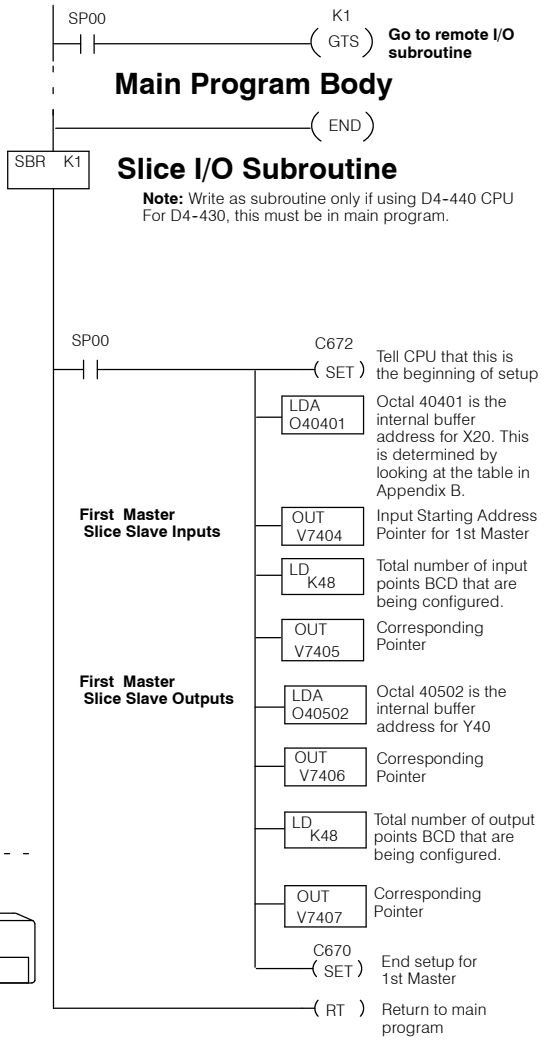
Set to: 153.6 kB

On Back

*In Chapter 3, you will learn how the setting of the binary switch on the master module affects the system's ability to make use of discrete addressing and the system's slave removal process.

Step 3: Write the Setup Program

RLL Program



Note: V-memory pointer for 1st Master inputs start at V7404 with number of points being transferred in V7405. The output pointer starts at V7406 with number of points being transferred in V7407.

If you were to use two channels, the second master pointers would be as follows: V-memory pointer for inputs would start at V7444 with number of points being transferred in V7445. Output pointer starts at V7446 with number of points being transferred in V7447.

A table showing all of the pointers is included in Chapter 4.

C670 ends the setup for 1st Master, but C674 must end the setup for 2nd Master.

2

Designing the Slice I/O System

In This Chapter. . . .

— Determine the System Layout
— Choose the Addressing Mode
— Complete the Programming Worksheets

Determine the System Layout

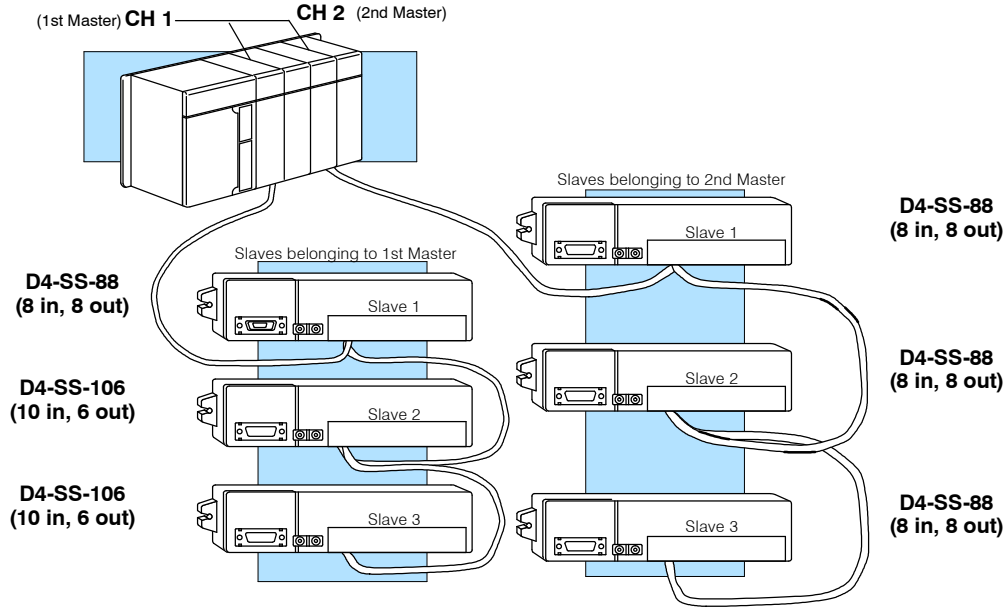
Determine I/O Needed and How Many Masters & Slaves

The first step in putting any system together is to at least establish a mental picture of the system components. You should determine the number of input and output points needed, which in turn will allow you to determine the number (and types) of slave units required. You may even want to draw a diagram.

An Example System

We'll use the following example system to help you understand these choices.

- Two channels to wire two different areas of some machine.
- Channel 1 uses 28 inputs and 20 outputs spread over three slave units
- Channel 2 uses 24 inputs and 24 outputs spread over three slave units



Choose the Addressing Mode

Once you have determined the number of I/O points, masters, and slave units required for your application, you have to choose the addressing mode. This allows you to assign the I/O points that will be used by each slave unit. You may recall that Chapter 1 provided a detailed description of the different modes. The following table provides a quick overview of each choice.

Addressing Mode	Ease of Programming	Slave Number Limitations	Special I/O Point Assignments	Number of Points Consumed	Availability
Automatic	Easiest	12 per master	Inputs start at X200 Outputs start at Y200	32 per slave (16 Input & 16 Output)	Can be used with 1 master only
Manual	Easy	15 per master	Any available addresses	32 per slave	Can be used with both masters
Discrete	Less Easy	7 per master	Any available addresses	Only the inputs and outputs needed per slave as long as it is in blocks of 8 pts. each	Can be used with both masters

32-Point I/O Consumption Rule

When you use either automatic or manual addressing, notice that a total of 32 I/O points are consumed for each slave (16 inputs and 16 outputs) regardless of how many I/O points are actually present on the slave. However, with the discrete addressing mode, the Slice slaves may not necessarily consume 32 I/O points. It depends on which Slice slave you're using. For example, with discrete addressing, the D4-SS-16N would only use 16 inputs and the D4-SS-16T would only use 16 outputs.

16-point Boundary Rule

With manual or discrete addressing you can specify the starting address and the data type (X, Y, C, etc.). *These addresses must be on a 16-point boundary.* For example, let's say you have a system that has consumed local base input points up through X27. Now let's say you want your first Slice slave to be a D4-SS-16N and you want to continue to use the X input data type for these points. You may think that your first address for this slave will be X30, which is the next input address following X27. However, X30 does not start on a 16pt. boundary. The next available input point for the Slice slave will be X40 in this example. (Remember, the DL405 uses octal addressing for the I/O points.)

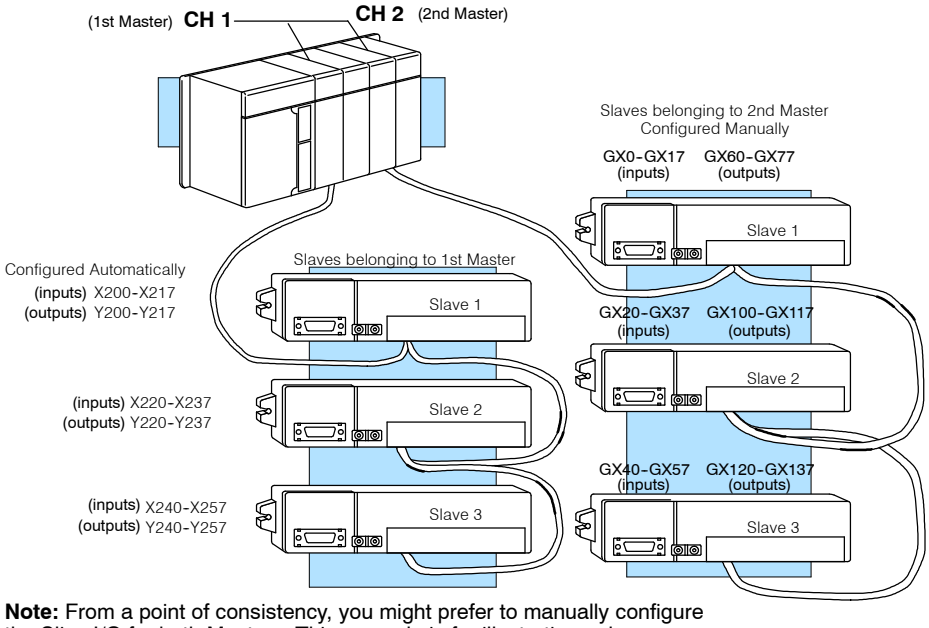
The setup routines described later actually help make sure this happens. You may recall that the CPU requires you to load an address into the pointer locations that setup the Slice I/O. These V-memory addresses automatically start on 16-point boundaries, so you cannot actually start the numbering incorrectly. This is just important when you're trying to determine your starting address.

Example System Addressing

In our example system, we have only used 3 slaves per master. This is well within the limit for each addressing mode, so we can choose from any of the options shown in the previous table. However, we decided to choose:

- Automatic addressing for Channel 1 (1st Master)
- Manual addressing for Channel 2 (2nd Master)

With these choices, our addressing assignments would be as shown in this diagram.



Note: From a point of consistency, you might prefer to manually configure the Slice I/O for both Masters. This example is for illustration only.

Remember, automatic addressing can only be used with one of the two possible masters in the CPU base. We could not, for example, have used automatic addressing in CH2 because we have already used it for CH1. You do not have to use automatic addressing at all if you prefer not to do so. For example, both of these channels could have been configured using manual addressing.

Other Examples

Here are a few more examples that may help you understand addressing choices.

Example 1: *You need a system with 12 slaves and you plan to use only one master. The rest of your system does not use any points assigned to either X200 (or above) or Y200 or above. You are not cramped for I/O points in your total system.*

Solution: Choose automatic mode. It takes just a few lines of ladder logic, and it allows up to 12 slaves per master. Although it can only be used with one master, you only have one master–so it's not an issue. You'll consume 32 points per slave, but you have plenty of I/O for your other needs.

Example 2: *You need 28 slaves in your system. What mode should you choose?*

Solution: You will have to use two masters and have manual addressing for both of them. It's the only way you can address more than 27 slaves.

Example 3: *You want to add a Slice I/O system that requires nothing but inputs at each slave station. You decide to use the D4-SS-16N for each slave location. You are going to need as many I/O points as possible for all of your local I/O.*

Solution: Use discrete addressing. This allows you to only consume 16 points at each slave station, instead of the usual 32 required for the other modes. You can have up to 7 slave stations per master, depending on needs and I/O address availability.

Complete the Programming Worksheets

Once you've determined the addressing mode and the address assignments, it is helpful to complete a programming worksheet to simplify the creation of the RLL setup program. In Appendix A of this manual you will find a blank Slice Slave Worksheet. We suggest that you photocopy this sheet and use it to map out the details of your system. Assuming this will be your procedure, this chapter will walk you through the worksheet by using the previous example system. You can use the details from these worksheets when you set the switches on your hardware and when you write any necessary setup logic.

Filling Out the Slice Slave Worksheet for the 1st Master

The following Slice Slave worksheet has been filled in for the 1st master module of the example system shown on the previous page.

Master Module No. 1

Slice Slave Worksheet

Unit Address	Model Name	INPUT		OUTPUT	
		Input Address	**No. Inputs**	Output Address	**No. Outputs**
1	D4-SS-88	X200	16 (only 8 used)	Y200	16 (only 8 used)
2	D4-SS-106	X220	16 (only 10 used)	Y220	16 (only 6 used)
3	D4-SS-106	X240	16 (only 10 used)	Y240	16 (only 6 used)
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					

Input Bit Start Address: X200 **V-Memory Address:V** N/A (automatic)

Total Input Points Consumed 48 **Input Points Used** 28

Output Bit Start Address: Y200 **V-Memory Address:V** N/A (automatic)

Total Output Points Consumed 48 **Output Points Used** 20

For the 1st master, we have decided to use **automatic addressing** for its slaves. This means that inputs (X's) and outputs (Y's) will be assigned starting at X200 and Y200 respectively. With automatic addressing we do not have to worry about looking up the V-memory addresses for the master module's internal memory and the slave I/O points, because the information is automatically mapped to the CPU's memory image area. Unlike manual or discrete addressing, you do not have to write ladder logic to setup the mapping process. This is why we have written "N/A" in the V-memory area of the form.

Now let's complete go to the next page and fill out a worksheet for the 2nd master.

Filling Out the Slice Slave Worksheet for the 2nd Master

The following Slice Slave worksheet has been filled in for the 2nd master of the example system.

Master Module No. 2

Slice Slave Worksheet

Unit Address	Model Name	INPUT		OUTPUT	
		Input Address	No. Inputs	Output Address	No. Outputs
1	D4-SS-88	GX00	16 (only 8 used)	GX60	16 (only 8 used)
2	D4-SS-88	GX20	16 (only 8 used)	GX100	16 (only 8 used)
3	D4-SS-88	GX40	16 (only 8 used)	GX120	16 (only 8 used)
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					

Input Bit Start Address: GX0 **V-Memory Address:V** 40000 ← **See Appendix B**

Total Input Points Consumed 48 **Input Points Used** 24

Output Bit Start Address: GX60 **V-Memory Address:V** 40003 ← **See Appendix B**

Total Output Points Consumed 48 **Output Points Used** 24

For the 2nd master, we have decided to use **manual addressing** for its slaves. This means you must use the tables in Appendix B of this manual to determine the master module's internal V-memory locations for mapping against the corresponding CPU's V-memory. In Chapter 4, we will show you how to write the ladder logic to setup the mapping process. Right now, you need only look at the table to find the master module's V-memory locations corresponding to points GX0 and GX60–the starting points for the inputs and outputs of our example.

We have used **global data types** here because of simplicity. If we had manually used X's and Y's, we would have had to be concerned with what X's and Y's were already being used by the modules in the local and/or expansion bases. With global assignments, you do not need this information. This is a particularly good characteristic when you think that the configuration of the other I/O in the base may be changed in the future, i.e. new modules added, removed, etc.

Now that the amount of I/O has been decided upon and you have determined how many masters and which slaves you will be using, you are now ready to do the installation and wiring. Chapter 3 will cover this in detail. Then, later, in Chapter 4, you will learn how to write the setup logic to actually tell the CPU how to assign these addressing choices.

3

Installation & Wiring

In This Chapter. . . .

Introduction

NOTE: It is advised that you read the previous chapter on "Designing the Slice I/O System" before you install your Slice master and slave units. The decision making process explained in that chapter will help you understand how you should set the rotary switches and dip switches on the units. It will also help you with writing your ladder logic in the next chapter.

6 Steps:

There are six steps to install master module and slave units:

1. Choose the baud rate by setting the dip switch on the rear of the master module and slave units.
2. Disconnect the power and insert the master module(s) into the CPU base.
3. Mount each of the slave units in their remote areas.
4. Set the address for each slave by using the rotary switch on the front of each slave unit.
5. Connect the communication cabling.
6. After making sure the power is turned off, connect the field wiring.

The following pages will cover each of these steps in detail.

This is all that is required to connect the masters and slaves. There are also optional features that you may want to use.

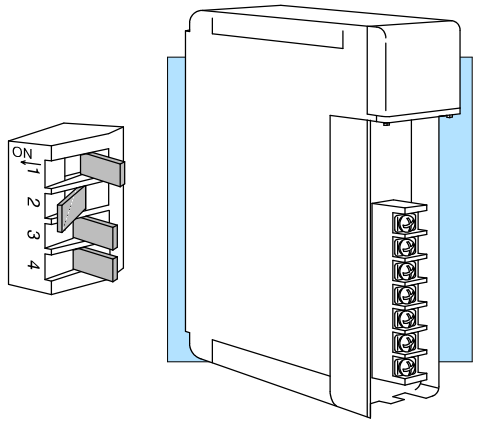
- Master unit Run Relay circuit
- Slave unit communications port

These topics are covered at the end of the chapter.

Step 1: Set the Baud Rate with the Rear DIP Switches

There are DIP switches on the rear of both the master and slave units. These switches must be set to the same baud rate. You have four choices, but whatever baud rate you select for the master, you must also use for its slaves. Use the table below for setting the switches. Also, if you chose discrete addressing when you designed your system, make sure you check switch 4 on the master. It must be turned on to enable discrete addressing.

Note that in this example, we have turned pos.1 to OFF and pos.2 to ON. 3 is not used and should always be set to OFF. This sets the baud rate to 153.6 kB. Position 4 is OFF unless you plan to use discrete addressing or the slave removal feature explained later.



Master

The settings of pos.1 and pos.2 of the slaves must match the ON/OFF state of these same positions on the master module's DIP switch. Otherwise, they will be set at different baud rates and will not be able to communicate.

Slave

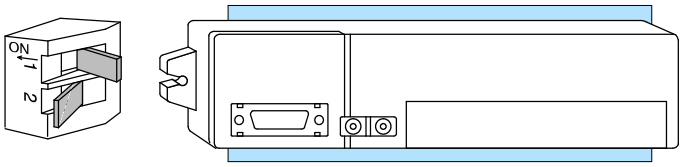


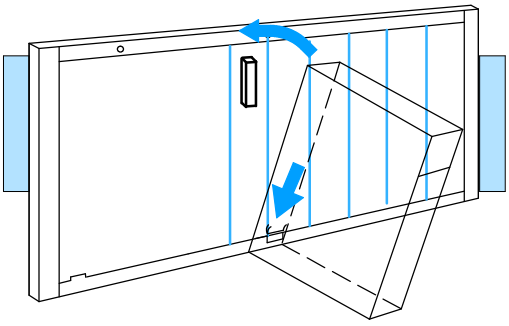
Table for setting DIP switch

Baud Rate		19.2kB	38.4kB	153.6kB	614.4kB
Master	**1**	OFF	ON	OFF	ON
	2	OFF	OFF	ON	ON
	3	Not used, should always be OFF			
	4	See Note	See Note	See Note	See Note
Remote	**1**	OFF	ON	OFF	ON
	2	OFF	OFF	ON	ON

Note: Position 4 of the Master enables or disables the system's ability to make use of discrete addressing or the automatic slave removal feature:
ON=Features enabled
OFF=Features disabled

Step 2: Install the Master(s)

You can install up to two masters in the CPU base. These can go into any available slot in the base.



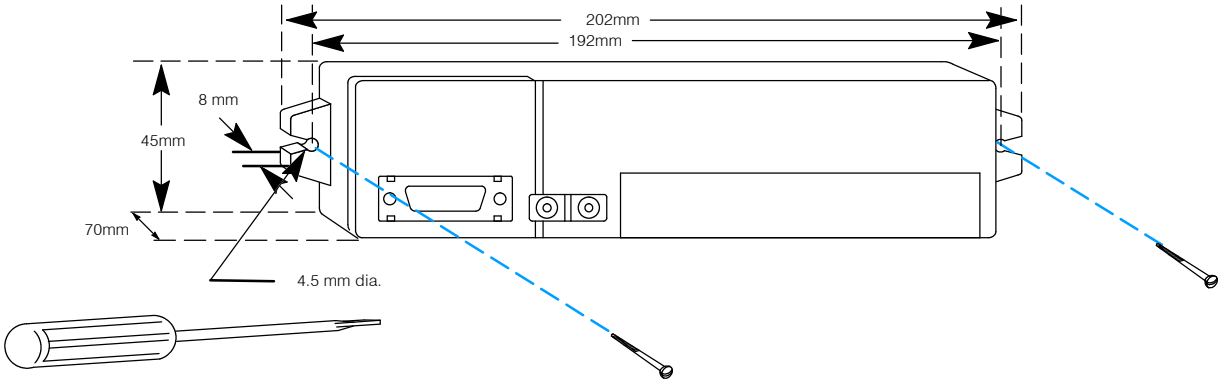
The master can go into any slot in the local base.

WARNING: To minimize the risk of electrical shock, personal injury, or equipment damage, always disconnect the system power before installing or removing any system component.

Notice the master module has plastic tabs at the bottom and a screw at the top. With the module tilted slightly forward, hook the plastic tab on the module into the notch on the base. Next, gently push the top of the module back toward the base until it is firmly seated into the base. Now tighten the screw at the top of the module to secure the module to the base.

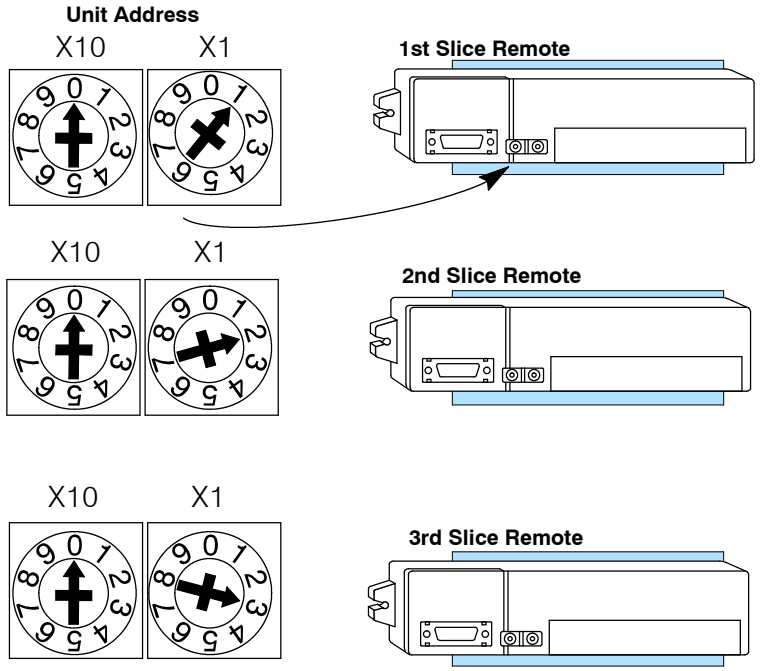
Step 3: Mount the Slave Units

Each slave unit is 202mm in width, 45mm in height and 70mm in depth. The slave units have flanges located on each side for using mounting screws to attach them to a wall or mounting plate. These mounting holes are located 192 mm apart (from center to center). The mounting screws do not come with the slave units. Remember that the slave units cannot be located more than 1000 feet from the local base.



Step 4: Set the Slave Address with the Front Rotary Switch

The Slice slave units have two small rotary switches on the front of their enclosure. One switch is marked X1 and the other X10. Don't confuse these with the conventional data type labeling--*these do not refer to inputs* X1 and X10. Instead, these set the unit address in decimal for each slave. X1 is the "one's" position and X10 is the "tens" position. For example, 13 is set by turning the X10 switch to 1 and the X1 switch to 3 (10 + 3 = 13). Since each Slice channel operates independently of the other, you start the unit addressing for the 1st Master's slaves at 01, and you start the unit addressing for the 2nd Master's slaves also at 01.



Align the arrow on the switch to any numbers between 01 and 15 (decimal), depending on which slave in sequence you are setting up and how many slaves are allowed per master Remember, each addressing mode (automatic, manual and discrete) has a particular limit on how many slaves can be connected to the master.

NOTE: Always use consecutive numbers for slaves and always start with Address 01 (not 00)--don't skip numbers.

Example Showing Proper Setting of Switches

Here's the way Steps 3 and 4 would be carried out for a system with one master and three slaves set to communicate at 153.6 kB:

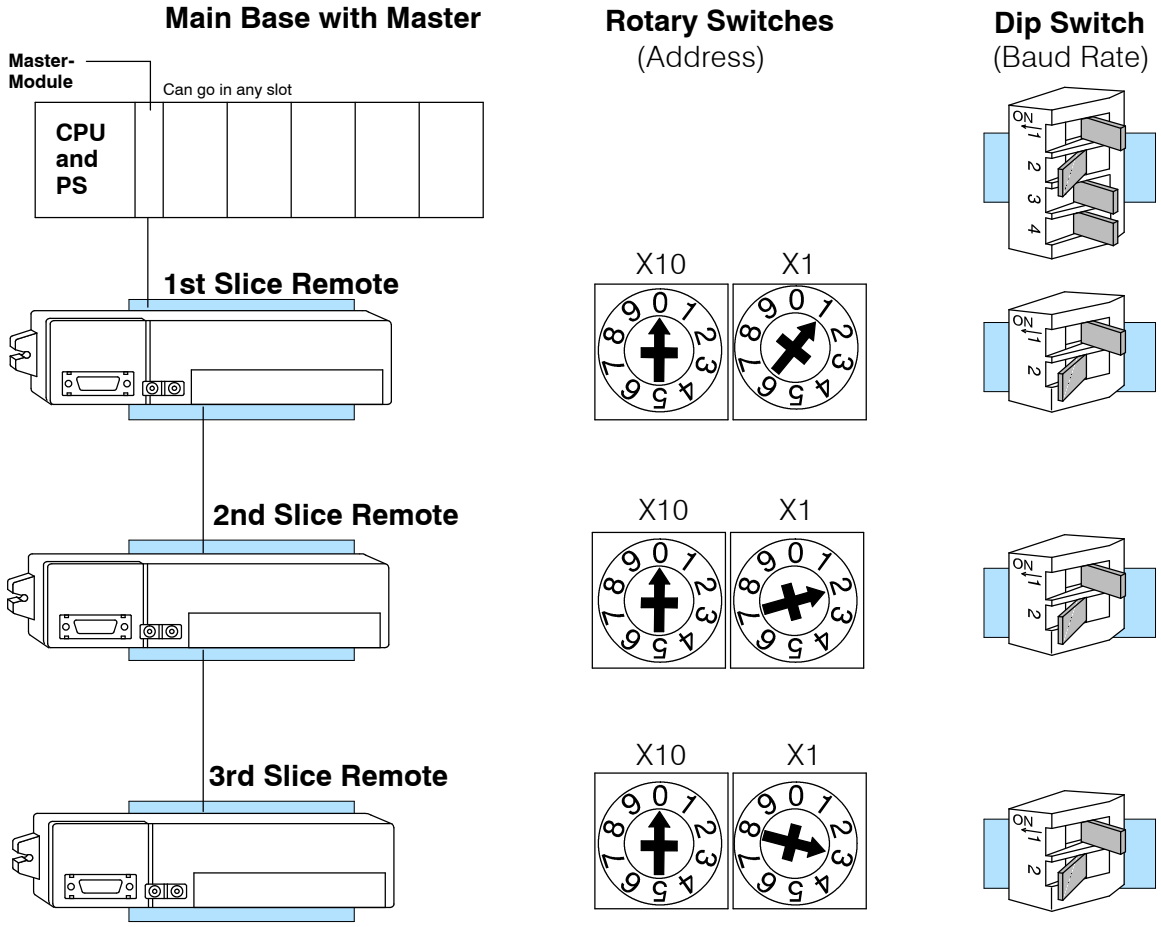


Table for setting DIP switch

Baud Rate		19.2kB	38.4kB	153.6kB	614.4kB
Master	1	OFF	ON	OFF	ON
	2	OFF	OFF	ON	ON
	3	Not used, should always be OFF			
	4	See Note	See Note	See Note	See Note
Remote	1	OFF	ON	OFF	ON
	2	OFF	OFF	ON	ON

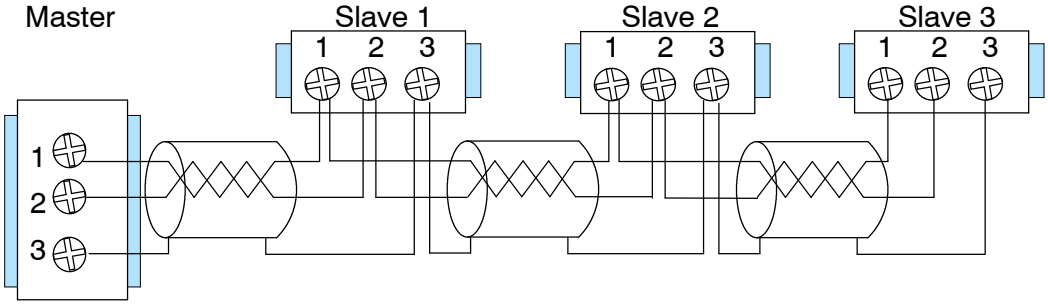
Note: Position 4 of the Master enables or disables the system's ability to make use of discrete addressing or the automatic slave removal feature:
ON=Features enabled
OFF=Features disabled.

Step 5: Connect the Communications Cable

Cabling Between the Master and Slaves

The following diagram shows the cabling between the master and its slaves. We recommend Belden 9841 or its equivalent for connecting the Master and Slaves. This is twisted pair cable. The two inner wires are connected to terminals 1 and 2 of each module. The shield wire is connected to terminal 3.

NOTE: *Do not connect the shield wire to the Ground terminal. Make sure the the connections between master and all slaves are always 1 to 1, 2 to 2 and 3 to 3.*



Termination Resistors

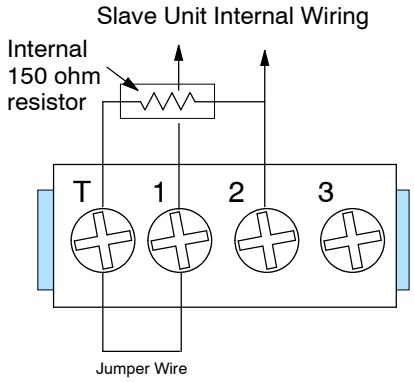
At each end of a master/slave system, it is necessary to have a "termination resistor" to prevent signal reflections from interfering with the communications. Although the modules have a 150 ohm resistor built in for this purpose, there are three options to consider.

- Use the internal resistor
- Use an external resistor
- Use an external resistor in series with the internal resistor.

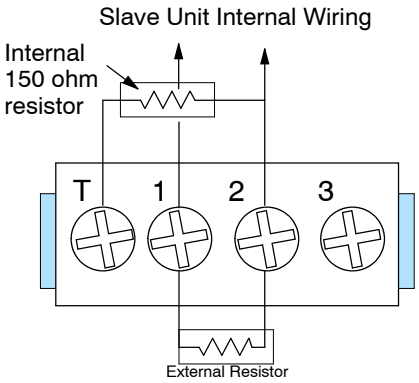
The following diagrams show these options in more detail.

Option 1:
Use Internal Resistor Only

With this configuration, you use the internal resistor of the module to provide all the terminating resistance necessary. A jumper wire is placed between the terminating terminal and terminal 1.

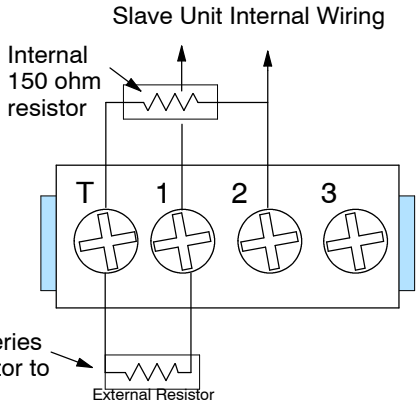


Option 2:
Use an External Resistor
To better match the impedance of the cabling, you can elect not to use the internal resistor; and instead, use an external resistor of your choice. This is connected between terminals 1 and 2. You **do not** use the jumper wire in this case.



You add your own resistor, using a resistor between 100 and 300 ohms to match the impedance of the cable.

Option 3:
External Resistor in Series
With this option, you use an external resistor in series with the internal resistor. The series resistance should match the cabling impedance.



Step 6: Connect the Field Wiring

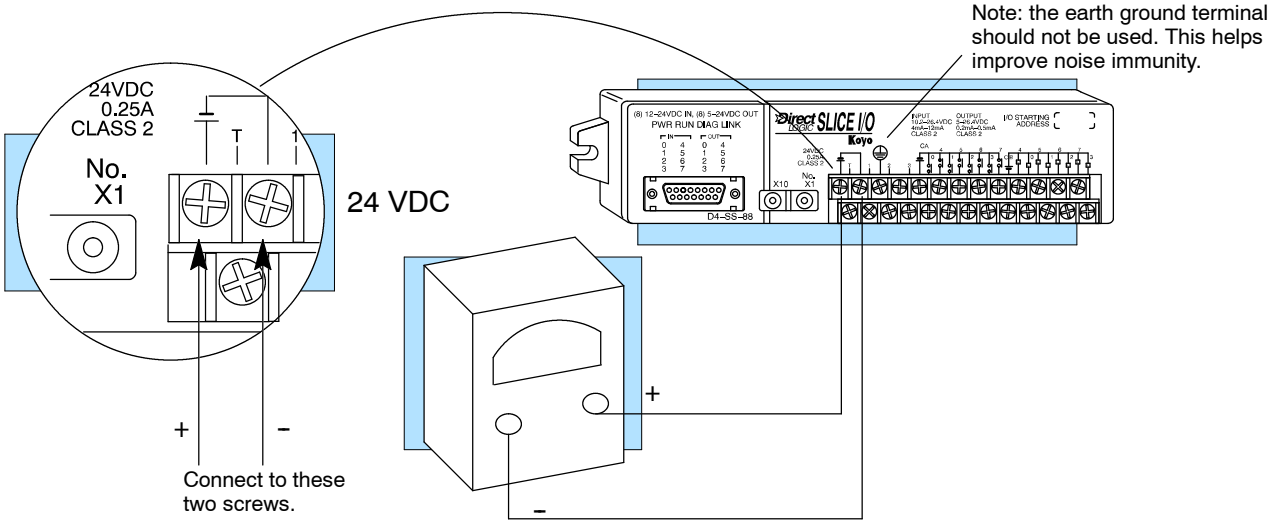
General Wiring Guidelines

You should consider the following wiring guidelines when wiring your system.

1. There is a limit to the size of wire the modules can accept. 16 AWG to 24 AWG is recommended. Smaller AWG is acceptable.
2. Always use a continuous length of wire, do not combine wires to attain a needed length.
3. Use the shortest possible cable length.
4. Where possible, use wire trays for routing.
5. Avoid running wires near high energy wiring.
6. Avoid running input wiring in close proximity to output wiring where possible.
7. To minimize voltage drops when wires must run a long distance, consider using multiple wires for the return line.
8. Where possible, avoid running DC wiring or communication cabling in close proximity to AC wiring.
9. Avoid creating sharp bends in the wires.
10. Label all wires.

Power Connections for the Master and Its Slaves

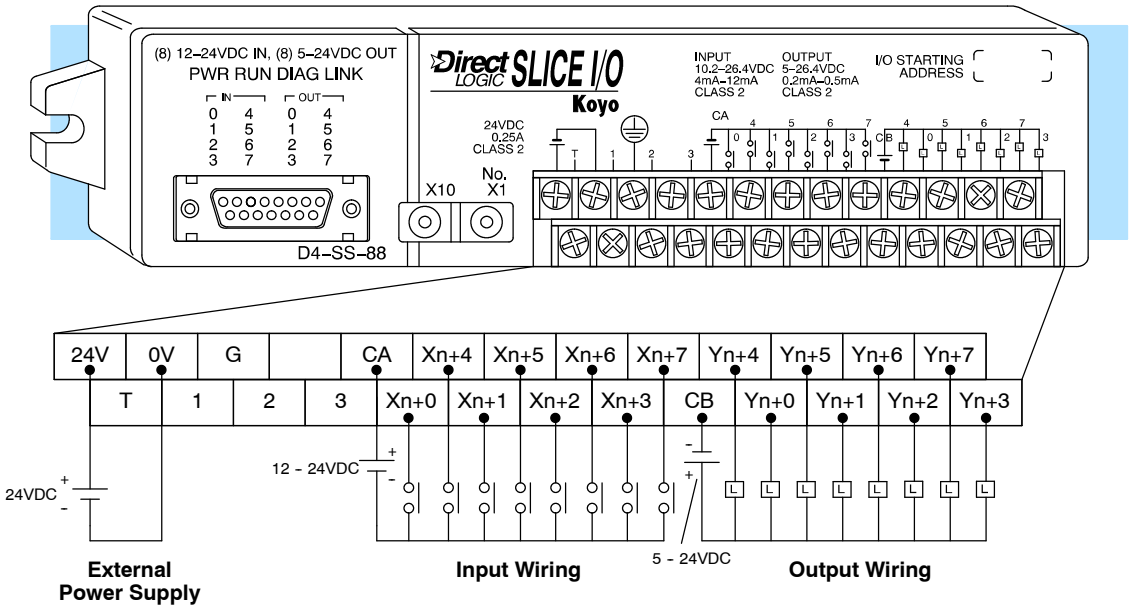
The master module is powered through the backplane of the local base. The slaves, however, require an external 24VDC power supply. *The Slave units will not operate unless this supply is connected.*



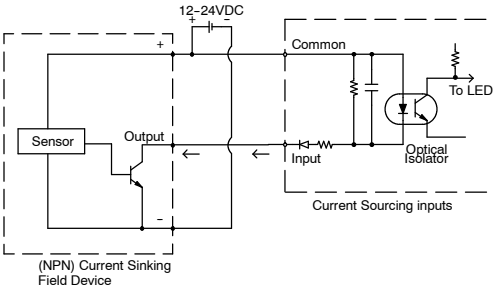
NOTE: If you are using 24VDC for your input and/or output field devices, it may be possible to use the above power supply for the field power as well. If you use the same supply, make sure you have calculated the maximum load required and that you size the power supply accordingly.

D4-SS-88 I/O Field Device Wiring Diagram

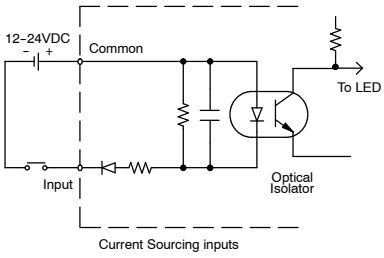
Use the following wiring diagram to connect the field wiring to the I/O terminal strip. The I/O point addresses have been labeled “Xn” and “Yn” to indicate the starting address. The X and Y data types have only been used for illustration purposes. Your exact starting addresses and data types depend on the addressing mode selected.



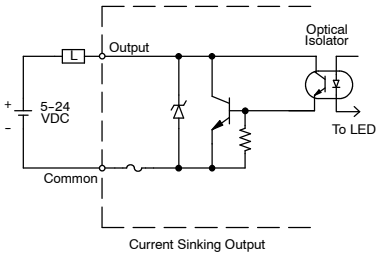
Solid State NPN Field Device Wiring



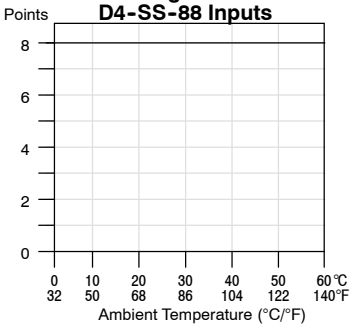
Typical Input Circuit



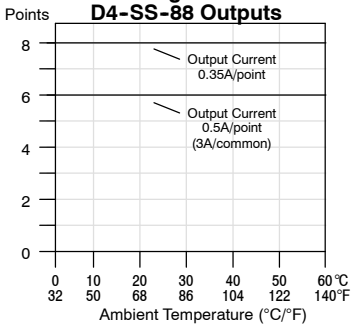
Typical Output Circuit



Derating Chart for D4-SS-88 Inputs

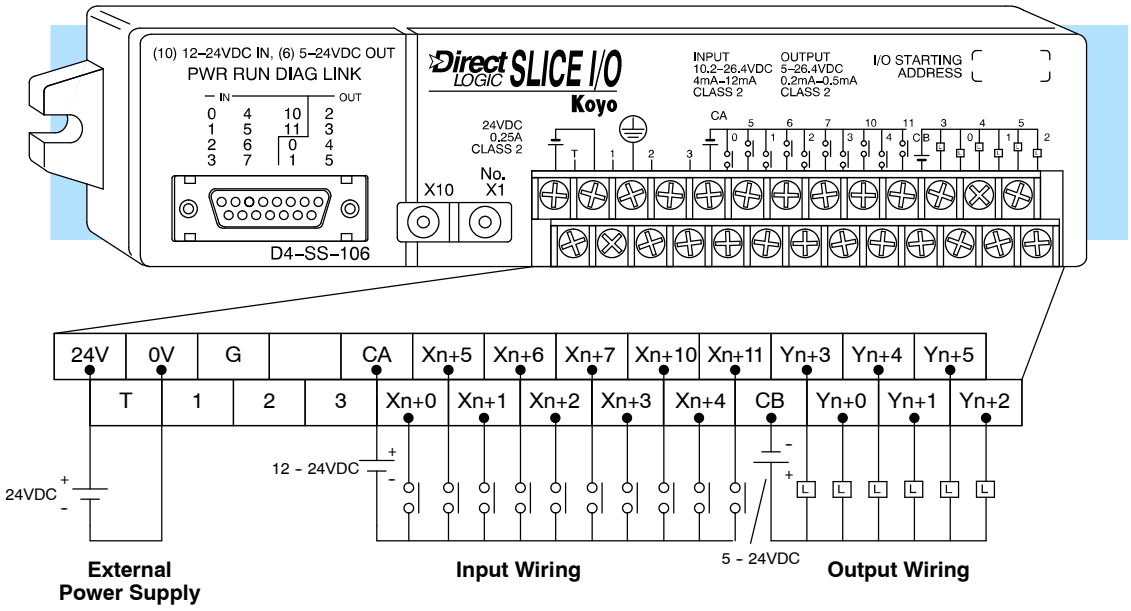


Derating Chart for D4-SS-88 Outputs

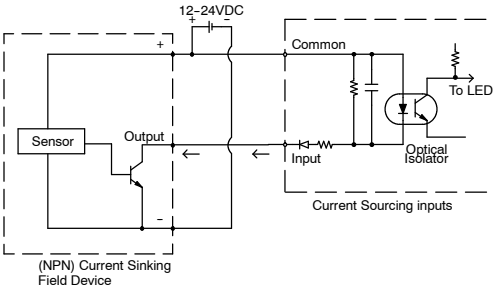


D4-SS-106 I/O Field Device Wiring Diagram

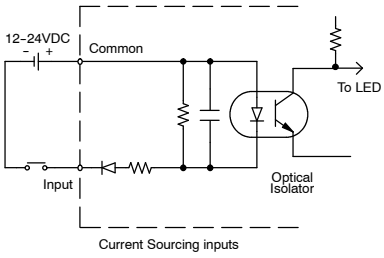
Use the following wiring diagram to connect the field wiring to the I/O terminal strip. The I/O point addresses have been labeled “Xn” and “Yn” to indicate the starting address. The X and Y data types have only been used for illustration purposes. Your exact starting addresses and data types depend on the addressing mode selected.



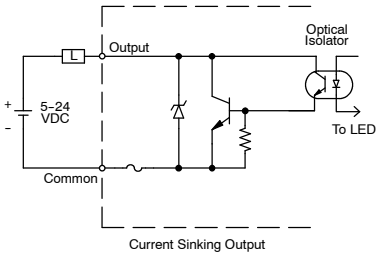
Solid State NPN Field Device Wiring



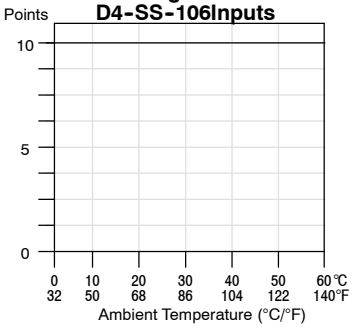
Typical Input Circuit



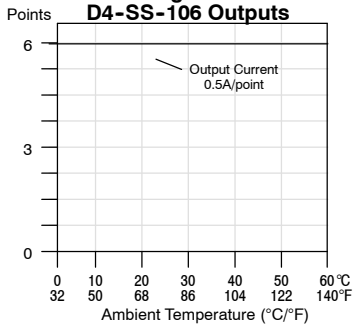
Typical Output Circuit



Derating Chart for D4-SS-106Inputs

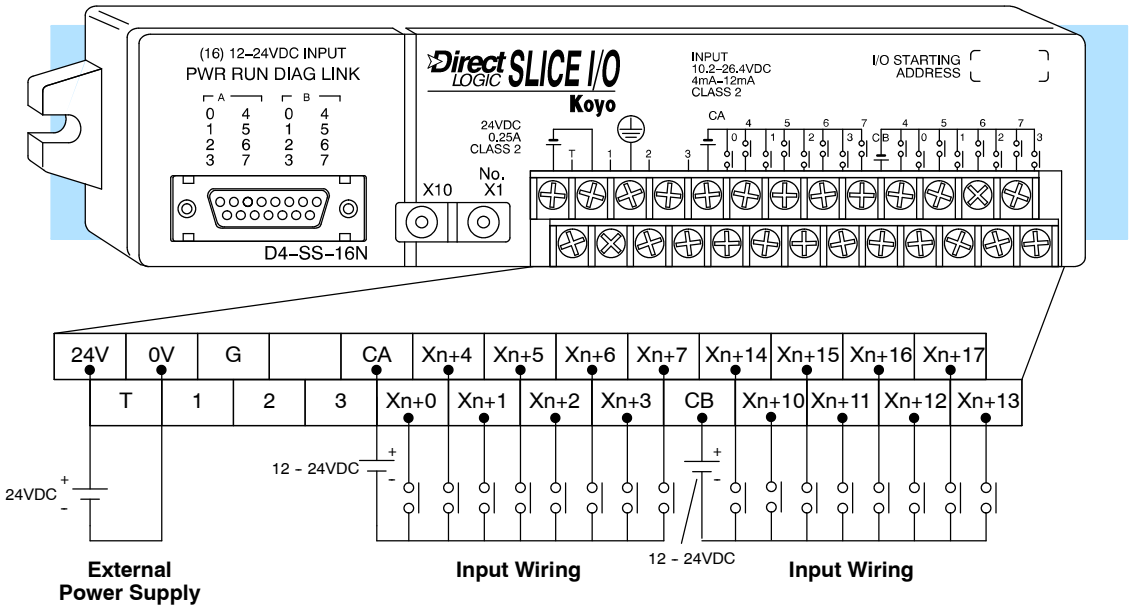


Derating Chart for D4-SS-106 Outputs

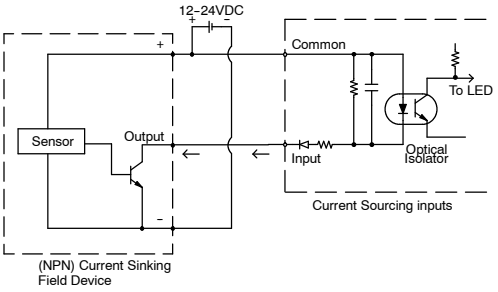


D4-SS-16N I/O Field Device Wiring Diagram

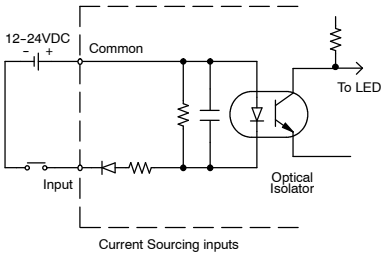
Use the following wiring diagram to connect the field wiring to the I/O terminal strip. The I/O point addresses have been labeled “Xn” and “Yn” to indicate the starting address. The X and Y data types have only been used for illustration purposes. Your exact starting addresses and data types depend on the addressing mode selected.



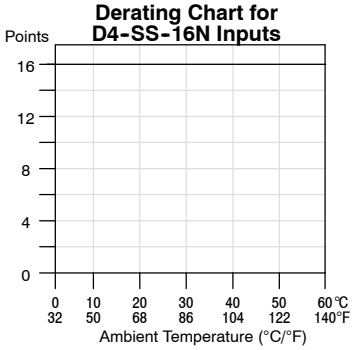
Solid State NPN Field Device Wiring



Typical Input Circuit

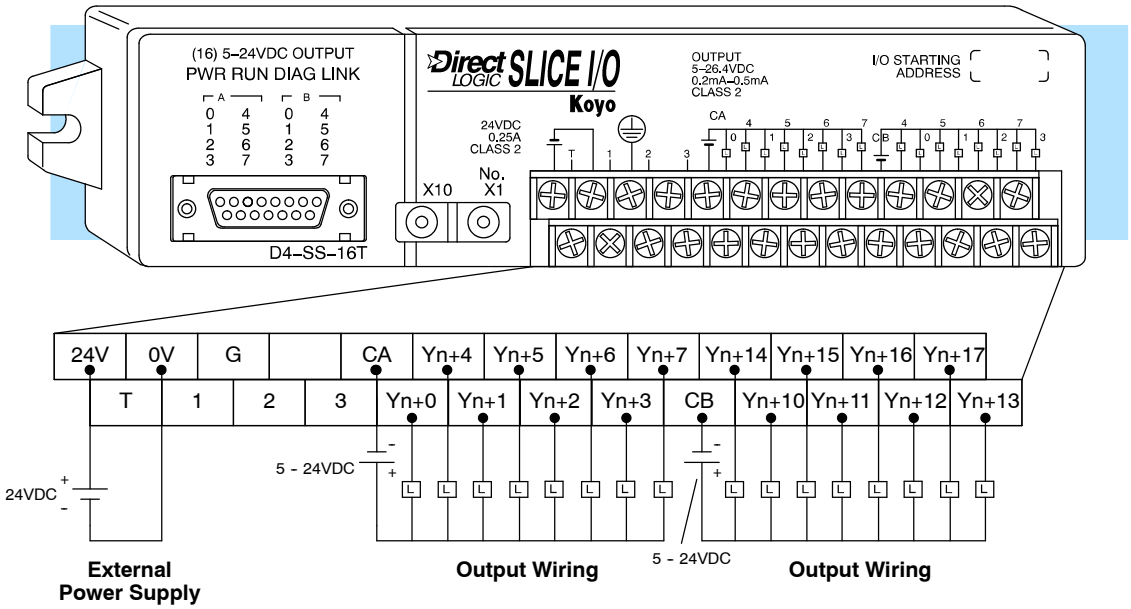


Derating Chart for D4-SS-16N Inputs

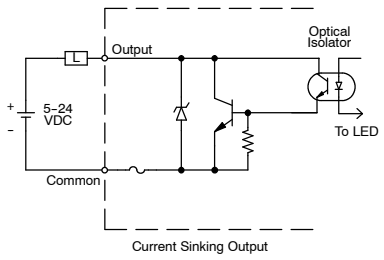


D4-SS-16T I/O Field Device Wiring Diagram

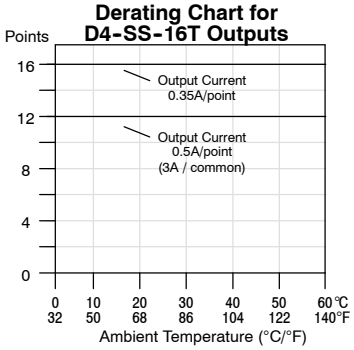
Use the following wiring diagram to connect the field wiring to the I/O terminal strip. The I/O point addresses have been labeled “Xn” and “Yn” to indicate the starting address. The X and Y data types have only been used for illustration purposes. Your exact starting addresses and data types depend on the addressing mode selected.



Typical Output Circuit



Derating Chart for D4-SS-16T Outputs

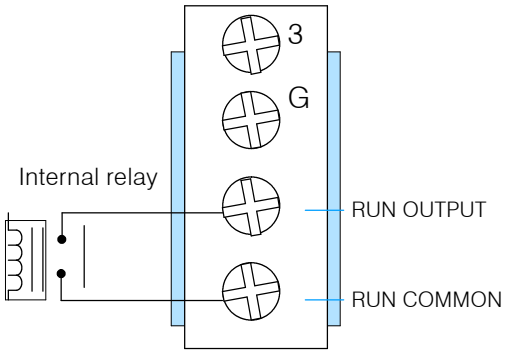


Optional Features

Connecting the Run Output Circuit

The master module has a normally open relay that closes when communication is successfully made between the master and its slaves. Each module has its own LED indicator (labeled "LINK")that glows if there is a communications error or no link.

The Run Output relay of the master module can be wired to a 24 VDC sinking input module so that ladder logic can be written to monitor the communications link. The bottom two terminals of the terminal block are where the wires are connected from the input module.



The Run Output relay can handle the following loads.

- 250VAC @ 1.0A
- 30VDC @ 1.0A

If the RUN relay in the master goes OFF, then the RUN relay in all of the slaves will turn off also.

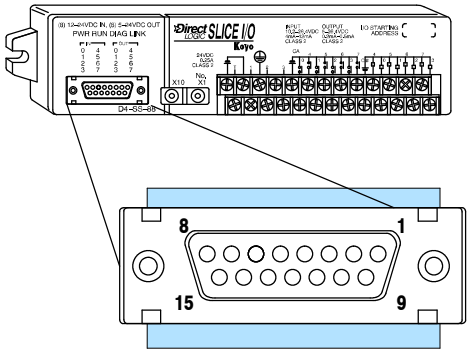
If you choose to wire an input (say, X10) from the Run Output, it is very easy to include a rung of logic to sound an alarm or to stop a process when a communication problem occurs:

Using the Slave Unit Communications Port

Each Slave unit has a 15-pin D-shell communications port. This port is the same as the top port on the DL405 CPUs. You can program or monitor the CPU through this port with ***Direct***SOFT or the handheld programmer. You can also connect the DV-1000 Operator Interface to this port. (Note, if you're using the handheld programmer or the DV-1000, remember to add the power requirement for the device when you select your 24VDC power supply.)

You can order the necessary cables with the following part numbers.

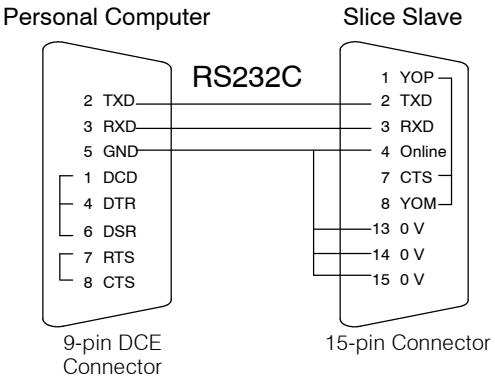
- **D4-DSCBL** — ***Direct***SOFT Programming cable for the DL405
- **D4-HPCBL-1** — DL405 handheld programmer cable (9.24ft., 3m)
- **D4-HPCBL-2** — DL405 handheld programmer cable (4.6ft., 1.5m)
- **D4-1000CBL** — DV-1000 cable (6.56ft, 2m)

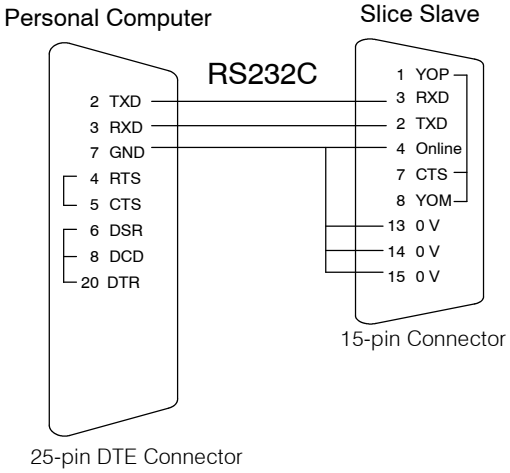


Pin numbers only shown for illustration

15-pin Female
RS232C
9600 Baud
8 Data Bits
1 Start Bit
1 Stop Bit
Odd Parity
Half-duplex
Asynchronous
DTE

Since the handheld programmer and the DV-1000 obtain their operating power from the Slave unit, we strongly suggest that you use the standard cables for these devices. However, there may be an occasion where you need to quickly make your own programming cable for use with your laptop or personal computer. In this case, use the following cable pinout diagrams.





Pin labeling conforms to the IBM DTE and DCE standards.

4

Writing the Setup Program

In This Chapter. . . .

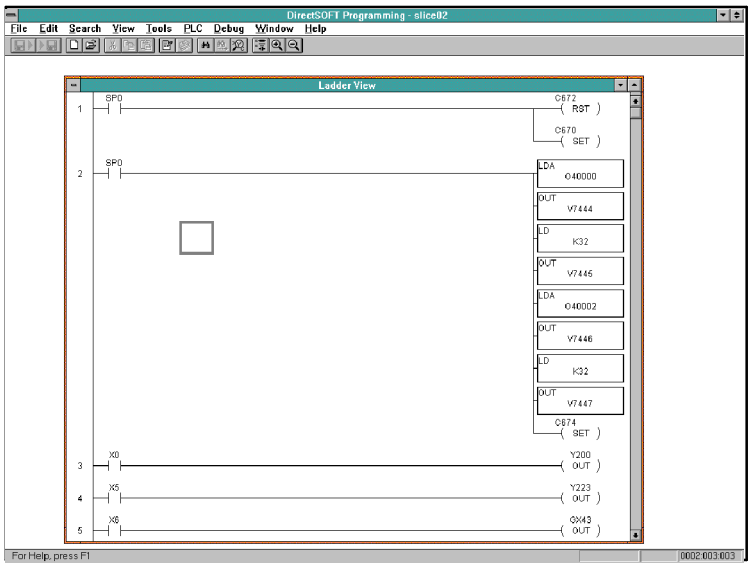
- Choosing a Programming Device
- Writing Your Slice I/O Setup
- Slave Removal
- Rejoining Slaves
- Special Relays Used for Slice I/O
- How to Use the Special Relays

Choosing a Programming Device

You can write your setup logic by using either a handheld programmer or our Windows-based ***Direct***SOFT programming software. It is generally much easier to use the software to generate the necessary setup logic. The examples that follow show the instructions in this format. Connect your computer through the CPU, and not through one of the slave units. Until you have completed the installation *and* the setup logic, you cannot communicate with the CPU via the slave unit communication ports.

To get started, enter ***Direct***SOFT and carry out the normal ***Direct***SOFT setup procedures for communicating with your DL405 CPU. If you do not know how to do this, refer to your ***Direct***SOFT Manual. Chapter 11 of your DL405 User Manual also has a very good explanation of the basic DL405 instruction set and examples of how these instructions are used for writing general ladder logic. In this chapter, we will only show you those instructions that are used to set up your Slice I/O system.

First open ***Direct***SOFT and establish a communication link with your CPU. Then enter the Edit Mode for programming. You should now be looking at a screen similar to the one shown below:



The ***Direct***SOFT window shown above depicts a program that has already been written. Of course, your programming window will be empty when you first open it. The following pages will show you how to write each part of your Slice I/O setup program.

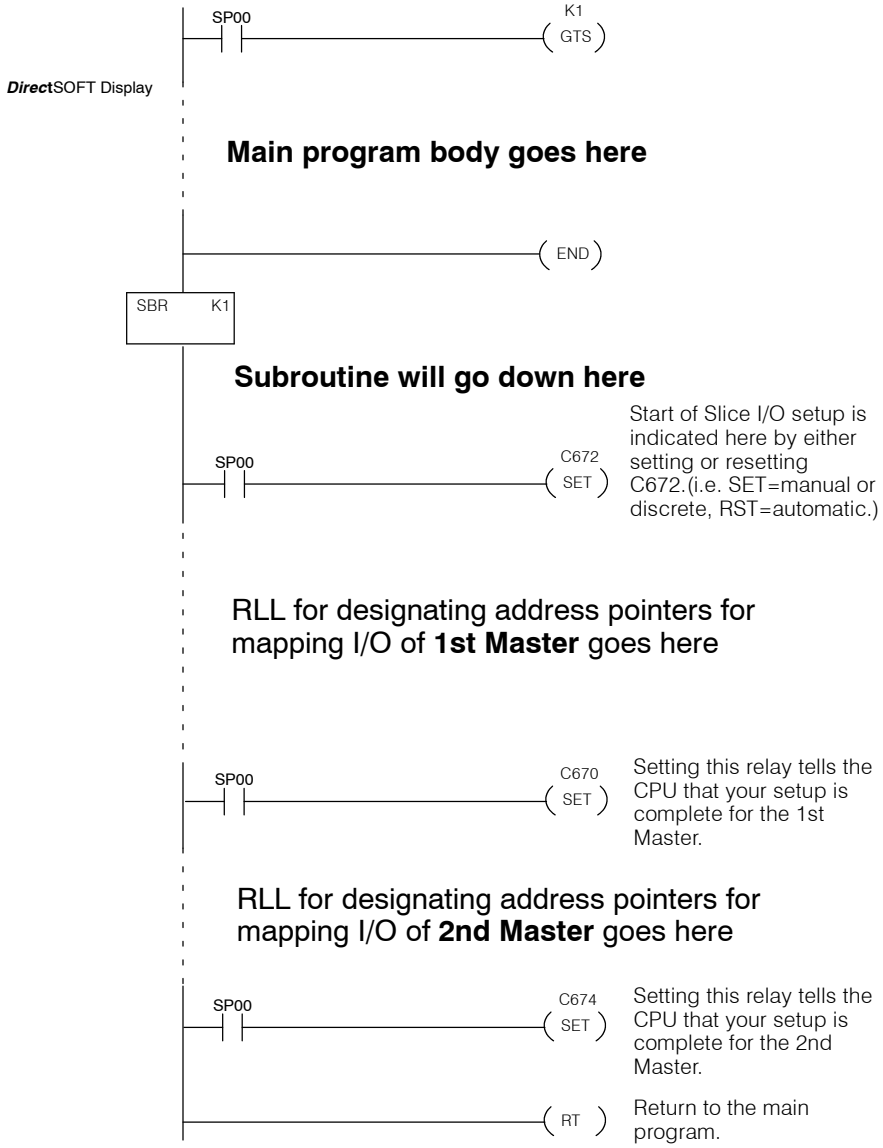
Writing Your Slice I/O Setup

Step 1: Decide How You Are Going to Execute Your Program

Is your setup logic going to be in the main program body or is it going to be in a subroutine? If you have a DL430, the decision is made for you. The DL430 does not support the subroutine instructions, so you have to put the setup logic in the main body of the program. The DL440, on the other hand, does support the subroutine instructions. The reason for using subroutines is because the setup logic only needs to be executed once. In the example below, we have suggested the use of SP00 so that the subroutine is only executed during the first scan. This means it will not impact the scan time on subsequent scans.

When you write your setup logic, it will be sandwiched in between rungs that affect the status of certain internal relays that are assigned to Slice I/O setup. These relays designate the beginning and end of your setup commands.

Sample RLL Structure for Slice I/O Setup



Step 2: Write the Setup Logic for Each Slice Master

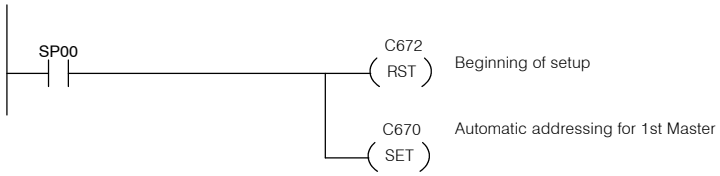
Whether you choose to write the Slice I/O setup program as a subroutine or as a part of the main program, the procedure is still the same. If you are using **automatic addressing** the process is very simple.

NOTE: You cannot use automatic addressing for both masters at the same time. If you want to use automatic addressing, you have to choose only one channel. Also make sure that the X's and Y's that are automatically assigned to the slaves are not used by the other modules in the system. Automatic addressing starts at X200 and Y200.

Automatic Addressing

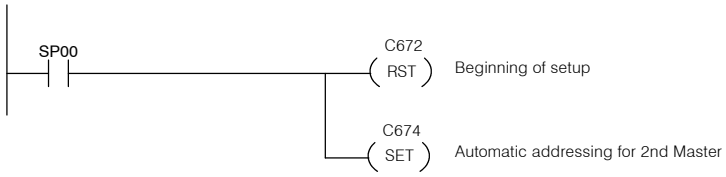
If you are using only one master module, then automatic addressing will probably be the only type of addressing you may ever need. Using *two* masters, however, produces some additional requirements. Automatic addressing can be used with either the 1st Master or the 2nd Master, but it can only be used with one of them in any given system. With automatic addressing, you do not have to assign the individual slave I/O addresses with your setup ladder logic because the CPU automatically assigns the data types (X and Y) and the respective addresses. You do, however, have to make sure that the C672 is set to zero (0) and that either C670 or C674 are set to one (1). If you are using automatic addressing with the 1st Master, then C670 must be set. If you are using automatic addressing with the 2nd Master, then C674 must be set. Switch #4 must be ON in order to use Auto Addressing.

Automatic Addressing Setup for 1st Master



The use of automatic addressing for the 2nd Master is essentially the same, except that you SET C674 instead of C670.

Automatic Addressing Setup for 2nd Master



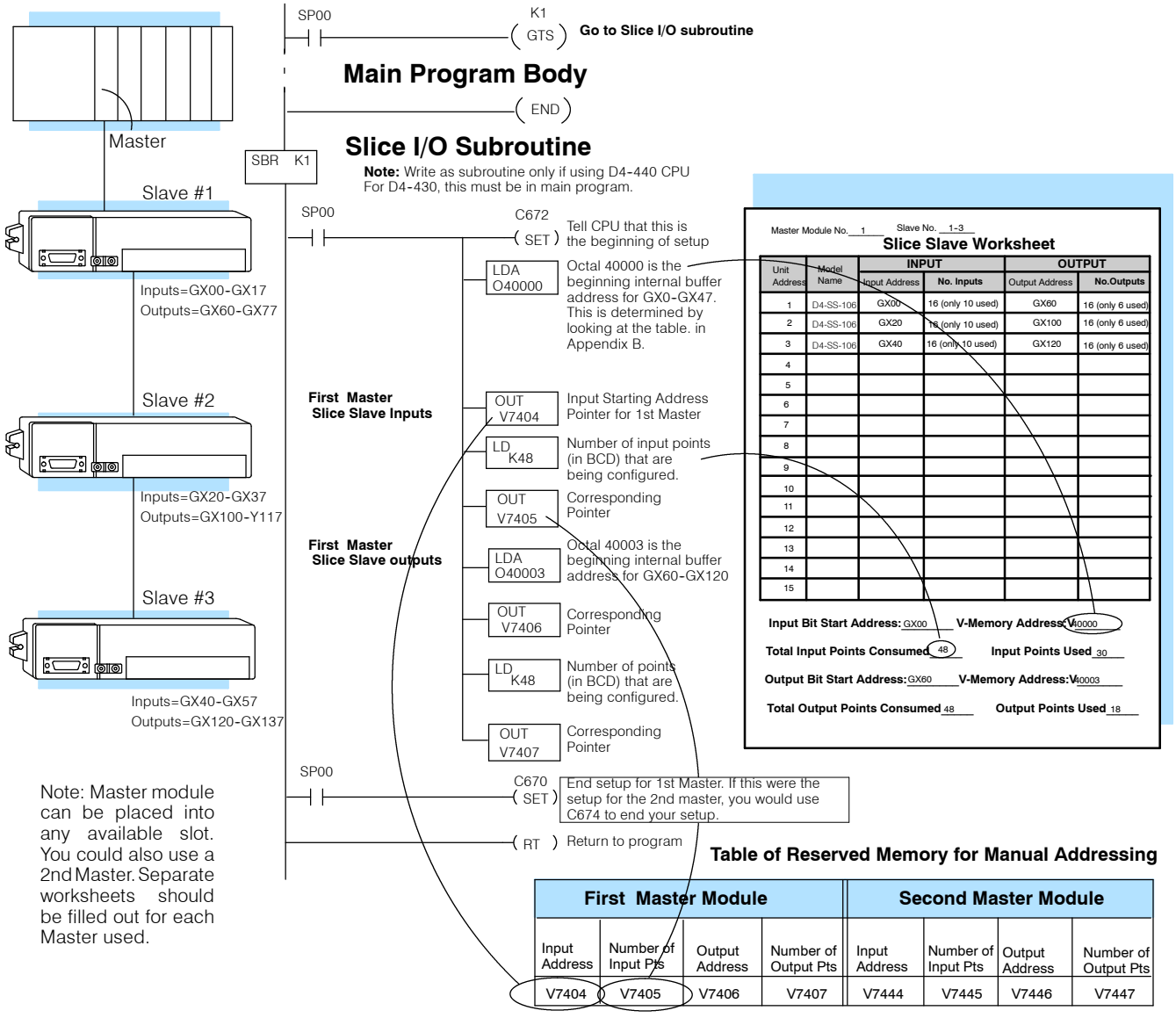
When the CPU detects one of the above setups in your ladder logic, it will assign slave inputs starting at X200 and slave outputs starting at Y200. It will consume 16 points for the inputs and 16 points for the outputs of each slave, regardless of which type of Slice slave you are using. For example, a D4-SS-106 will consume 16 input points and 16 output points, even though the slave does not have that many I/O points available. **You may have up to 12 slaves for the corresponding master when using automatic addressing.**

How About the Other Types of Addressing?

With manual or discrete addressing, you have some additional steps. In these cases, you have to write ladder logic that tells the CPU which addresses and data types you want to use. The CPU has predefined memory locations, called pointers (V74xx), that you can use to accomplish this task. Simply use the tables in Appendix B to find the V-memory location (V40xxx) that corresponds to the data type and address that you want to use as the starting address. Then, you can use the setup logic shown in the following examples to load these V-memory addresses into the pointers that the CPU uses to determine the Slice I/O point addresses. By doing this, your setup logic merely tells the CPU where to store the slave I/O points in the CPU image register area.

Manual Addressing

With manual addressing, you may use up to 15 slaves per channel. The following example system only uses 3 slaves. We have decided to use global GX data types in this example for our inputs and outputs. If you completed worksheets for your system, simply transfer the worksheet data as shown here. Also, if you examine this setup program, you'll notice that the V40xxx addresses have been properly designated as shown in Appendix B. The table at the bottom of the page is used for finding the CPU's V74xx pointer addresses.



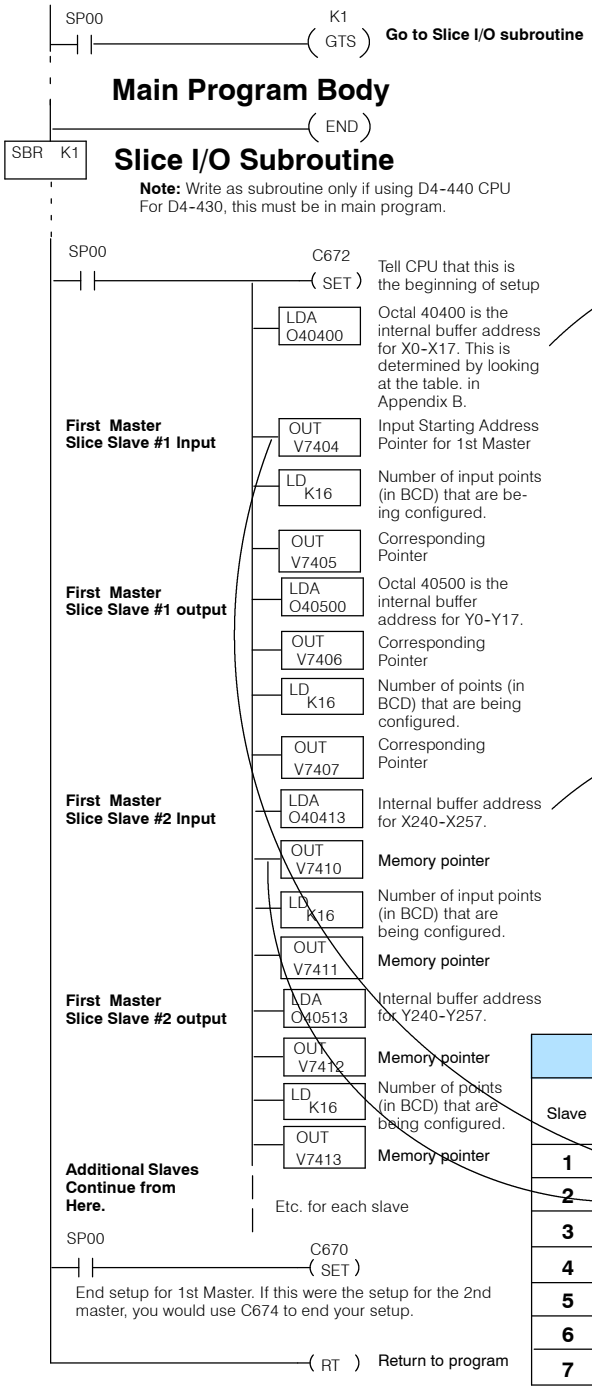
Note: Master module can be placed into any available slot. You could also use a 2nd Master. Separate worksheets should be filled out for each Master used.

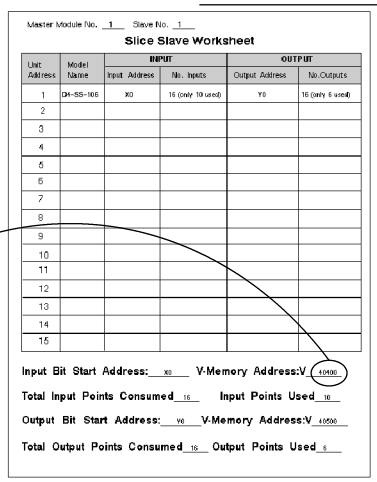
Table of Reserved Memory for Manual Addressing

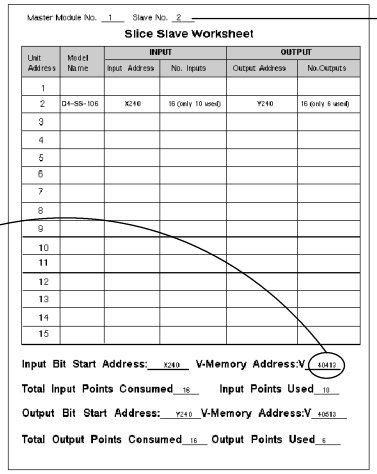
First Master Module				Second Master Module			
Input Address	Number of Input Pts	Output Address	Number of Output Pts	Input Address	Number of Input Pts	Output Address	Number of Output Pts
V7404	V7405	V7406	V7407	V7444	V7445	V7446	V7447

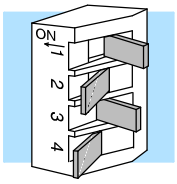
Discrete Addressing

The example shown below takes the same system shown on the previous page and uses *discrete* addressing. Notice that it uses an *expanded* reserved memory table for the CPU pointers and notice that **each slave is setup individually**. Also, the starting addresses can be out of sequence. In the example, we have used X0–X17and Y0–Y17 as the starting addresses for Slave #1 (V40400, V40500) and X240–X257 and Y240–Y257 as the starting addresses for Slave #2 (V40413, V40513). We have not shown Slave #3, but it could use any unused addresses from the X, Y, C, or GX tables, as well as be out of sequence. With this method, It's best to use separate worksheets for each slave. **You may have up to 7 slaves per master when using discrete addressing**.









Remember: You must set Pos.4 of the DIP switch to ON in order for discrete addressing to be available.

Note: Additional worksheet would be completed for Slave#3

Table of Reserved Memory for Discrete Addressing

	First Master Module				Second Master Module			
Slave	Input Address	Number of Input Pts	Output Address	Number of Output Pts	Input Address	Number of Input Pts	Output Address	Number of Output Pts
1	V7404	V7405	V7406	V7407	V7444	V7445	V7446	V7447
2	V7410	V7411	V7412	V7413	V7450	V7451	V7452	V7453
3	V7414	V7415	V7416	V7417	V7454	V7455	V7456	V7457
4	V7420	V7421	V7422	V7423	V7460	V7461	V7462	V7463
5	V7424	V7425	V7426	V7427	V7464	V7465	V7466	V7467
6	V7430	V7431	V7432	V7433	V7470	V7471	V7472	V7473
7	V7434	V7435	V7436	V7437	V7474	V7475	V7476	V7477

Slave Removal

Why Would You Use Slave Removal?

There are certain types of applications where you might want slave stations to be temporarily "logged out". Or, there may be some point in the process where you want to permanently remove one or more slaves. You may also want a slave to be disconnected when there is any sort of communications error. Of course, you do not want to disrupt anything else during the removal. This is when you need the slave removal feature.

What is It?

The slave removal feature allows you to remove a slave "on the fly", and even add it back to the system later. This can be triggered specifically in your program or it can occur upon detection of an error in the system. When slave removal is accomplished, the outputs for that slave go to zero (0) and the inputs are no longer read by the CPU.

Types of Slave Removal

You have a choice between two types of slave removal:

- **Manual Slave Removal**--At any point in your program, you can tell the CPU to ignore the I/O points of a particular slave. There does not have to be an error to trigger this feature.
- **Automatic Slave Removal**--This mode is triggered only by the occurrence of a Slice I/O error for the slave unit designated.

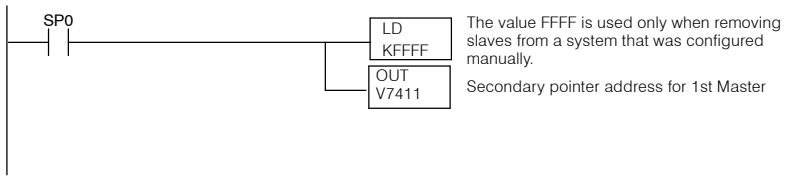
Don't confuse the use of the words "automatic" and "manual" here with our earlier reference for addressing modes. The terms here refer only to *slave removal*. For example, you can *manually* remove a slave from a system that has been *automatically* addressed. You can also automatically remove a slave from a system that has been manually addressed. With the one exception covered in the bottom paragraph, your addressing mode for your slave I/O points has nothing to do with slave removal.

How Pointer Addresses are Used for Slave Removal

The slave removal feature has "primary pointer" and "secondary pointer" setup locations. The *primary pointer address* is a V-memory assignment that is dependent on which type of slave removal is being used (manual or automatic)and the location of the master in the base (which slot). In a moment, we will show you a table of addresses so that you can determine where the primary pointers are located.

The *secondary pointer* address is always V7411 for the 1st Master and V7451 for the 2nd Master. **If you are removing slaves from a configuration that was addressed using manual addressing, the secondary pointer address must have hexadecimal FFFF written to it.** In all other cases, these addresses can have any number written to them **except** FFFF. Below is a sample segment of RLL that shows FFFF being written to the secondary pointer address of the 1st Master for a system that had its I/O points addressed manually.

Sample Logic for Writing to Secondary Pointer



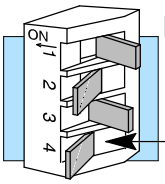
4 Steps for Using Slave Removal

Use the following steps to make use of the slave removal function:

1. Properly set the DIP switch on the rear of the master(s).
2. Determine the binary bit pattern for slave removal.
3. Determine the setup pointer for storing the bit pattern from Step 3.
4. Write the slave removal setup program.

Step 1: Setting the DIP Switch

Slave removal is only possible when you have placed Position 4 of the master module's DIP switch to ON.



DIP switch of Master Module

Must be placed in the ON position.

Step 2: Determining the Bit Pattern for Slave Removal

To remove a slave from the system, you set the bits in a 16-bit block according to the scheme shown below. This pattern must be converted to hex for programming.

How the Bits are Set to Designate Which Slaves to Remove

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Slave No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

Not used for manual removal
Set this bit to 1 to automatically remove any slave that has a communication problem.

Example for removing Slaves 1, 3, and 5:

Slave / bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**1**	**0**	**1**	**0**
	8	4	2	1	8	4	2	1	8	4	2	1	8	4	2	1
Hex		0				0				2				A		

Since the Bit number is the same as the Slave number, it is easy to know which bits to set. Once you set these bits, you can convert the binary value to hex. Notice how bits 1 and 3 result in 10, which is hex A.

Hexadecimal 2A

Step 3: Determining the Setup Pointer for Storing the Bit Pattern

The table shown below gives the pointer address for setting up the slave removal. Notice that the addresses vary according to the slot occupied by the master or masters, as well as the type of removal being used.

Slot	V-memory for Manual Removal	V-memory for Automatic Removal
0	V7660	V7670
1	V7661	V7671
2	V7662	V7672
3	V7663	V7673
4	V7664	V7674
5	V7665	V7675
6	V7666	V7676
7	V7667	V7677

Example:

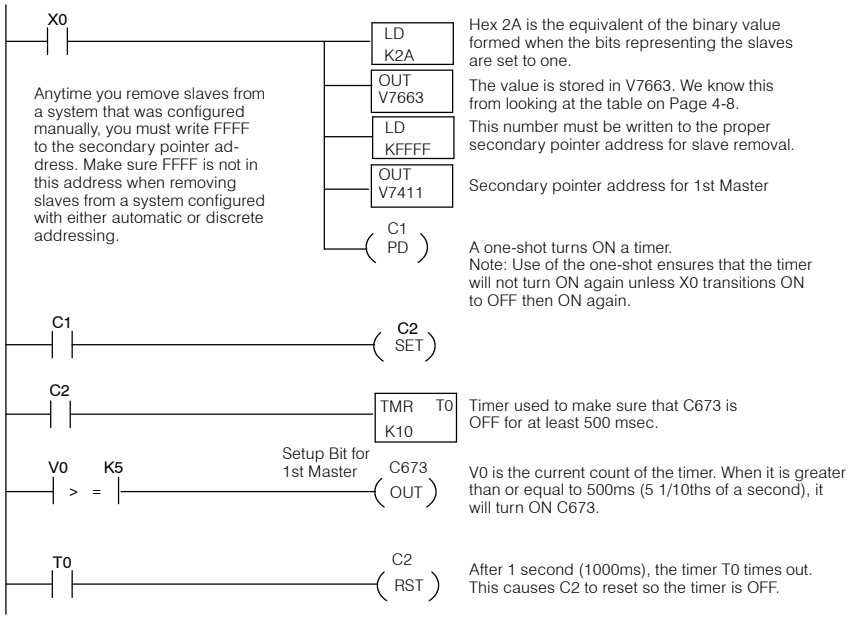
If we are using Manual slave removal and the Master is in Slot 3..

We would store the hex number representing the slave or slaves being removed in V7663.

Step 4: Write the Slave Removal Setup Program

The ladder logic is only slightly different for manual and automatic slave removal. Anytime you are using **manual slave removal**, the last few commands of the setup must transition either C673 or C677 OFF(for at least 500ms) and ON (for at least 500ms). C673 is used for the 1st Master and C677 is used for the 2nd Master. In the example below, we have used a one-shot and a timer to make sure we hold the OFF and ON states for the proper amount of time. We have decided to remove Slaves 1, 3, and 5 for the 1st Master when an ON signal is received from X0. This example configuration, by assumption, had its I/O points configured using manual addressing.

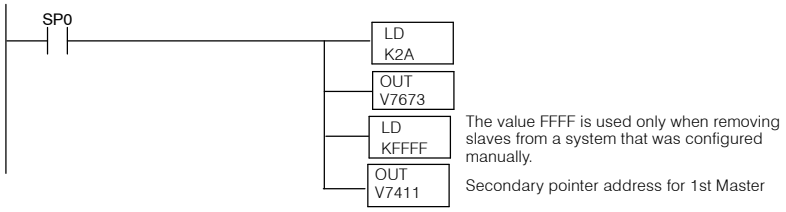
Sample Ladder Logic for Manual Slave Removal



Sample Ladder Logic for Automatic Slave Removal

Using the the same master and slaves of our example, let's take a look at how you would setup the **automatic removal of a slave**. Notice three differences:

- You use SP0 to setup the slave removal on the first scan.
- The V-memory is found on the right-hand side of the table (Page 4-8).
- There is no setup bit (such as C673 or C677) used.



NOTE: Remember, when you determine the bit pattern value for **automatic slave removal**, you have the option of merely setting Bit 0. This would indicate that you want *any* slave to drop out when it causes a communications error. If you do this, then you won't have to set each slave bit individually. In the above example, we only remove slaves 1, 3, and 5. Therefore, we decided not to use Bit 0. We instead set Bits 1, 3, and 5 which resulted in the value HEX 2A.

Rejoining Slaves

What is It?

After removing a slave, usually the application will call for the slave to be brought back on-line with the system.

How is It Done?

In the case of automatic slave removal, the rejoining of the slave or slaves is automatic. That is, as soon as the communications error is cleared, the removed slave or slaves will be brought back on-line. You don't have to write any logic.

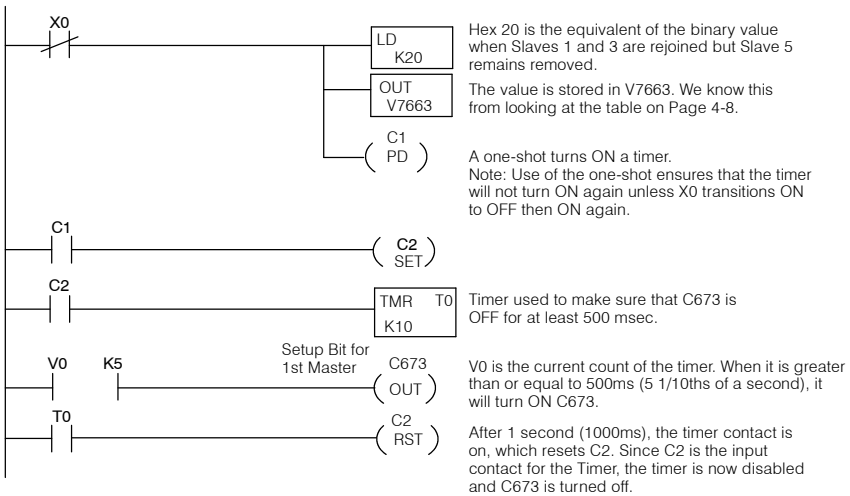
In contrast to this, when slaves have been manually removed from the system, you must write special ladder logic in order to bring them back on-line. There are two steps for doing this:

1. Change the bit pattern in the primary pointer address so that zeros (0) are in every bit position where you want a slave rejoined. Leave 1's in the bit positions where you have slaves removed that you wish to remain removed.
2. Transition the setup bit (C673 or C677) from OFF (at least 500ms) to ON (at least 500ms).

NOTE: The rejoining process causes the CPU to look at the bit pattern in the primary pointer address and REJOIN any slave that has a corresponding bit that is 0, and REMOVE any slave that has a corresponding bit that is set to 1. For example, if you write a zero to bit 3 in order to rejoin Slave 3, but you have bits 6 and 7 with ones stored at the time you transition the setup bit (C673 or C677); then, Slave 3 will be rejoined but Slaves 6 and 7 will be removed. If you don't want any slaves removed when you rejoin one or more slaves, then make sure that all 0's are written to the primary pointer address.

Example of Rejoining a Slave

Here's an example of rejoining Slaves 1 and 3 to a Slice I/O configuration where Slaves 1, 3, and 5 were previously removed. This means the bit pattern would be hex 20 because Bit 5 would still be a 1 and all the other bits would be 0's.



Special Relays Used for Slice I/O

The Slice I/O system has several relays that are used with your system. Some of these relays can be used in RLL routines that will detect and solve errors as a troubleshooting tool. In some cases (i.e. C700, C720, C710,C730), you can use ***Direct***SOFT to look in corresponding V-memory addresses for more information on the error. The following table lists all of the special relays assigned for Slice I/O.

Function of Relay	First Master Relay (s)	Second Master Relay (s)	Description
End of Setup	C670	C674	When set, these relays signify the end of the setup for all addressing modes.
Clear I/O on Error (Automatic Slave Removal)	C671	C675	These two relays are for determining whether you want the remote input points to be set to zero when an error occurs, or whether you want to freeze the current input status. If the relay is set, all the input points are cleared when an error occurs.
Beginning of Setup	C672	C672	When used in your ladder logic, this relay indicates that you are beginning your setup of the addressing for a Slice I/O system. If this relay is set to 1, the CPU knows to use manual or discrete addressing. If it is reset to 0, the CPU knows to use automatic addressing.
Activate Removal or Rejoining of Slaves	C673	C677	When transitioned from OFF to ON these relays will either remove or rejoin slaves depending on what is stored in the primary pointer address.
Communication Error	C700	C720	Automatically set by the CPU when there has been a communication error. Check the individual bits at V7700 to find out if the 1st Master or any of its slaves are responsible. Check the bits at V7701 to find out if the 2nd Master or any of its slaves are responsible. A 1 in bit 0 of either V-memory location means the master has been setup wrong (i.e. baud rate does not match its slaves). A 1 in any of the other bits indicates that there is either no response from the corresponding slave or the slave has failed a data test.
Mapping O.K.	C710	C730	Check the individual bits at V7702 to find out which slaves of the 1st Master have been mapped properly. Check V7703 for the mapping of the 2nd Master's slaves. If correct, there is a 1 in each bit position where there is an active slave.

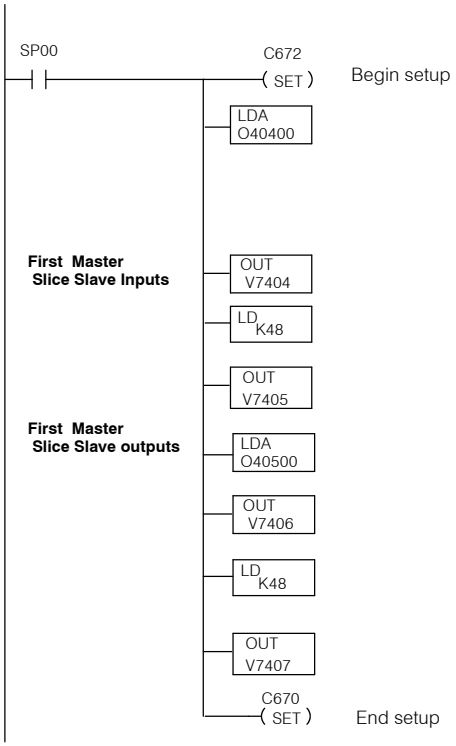
How to Use the Special Relays

C672/C670/C674

Here are some example uses of these relays and an added explanation for each of the relays discussed on the previous page:

These are setup flags for **marking the beginning and end** of your ladder logic that sets up your Slice I/O configuration. C672 marks beginning of all addressing logic. C670 is for ending setup for the 1st Master and C674 for the 2nd.

Example: Begin/End Setup for Manual Addressing of 1st Master



C671/C675 I/O Status On Error

C671 is assigned to the 1st Master. C675 is assigned to the 2nd Master. When any master can't talk to one or more of its slaves, the "link" LED will come on to indicate that there is a problem. The system will stop updating the remote I/O status in the CPU for that slave unit. You have several options at that point. One such option is either to **freeze the last known input status** that is in the CPU's memory image area, or to **write a zero to each point**. If these flags are OFF when the error occurs, all inputs will be zeroed.

Example:

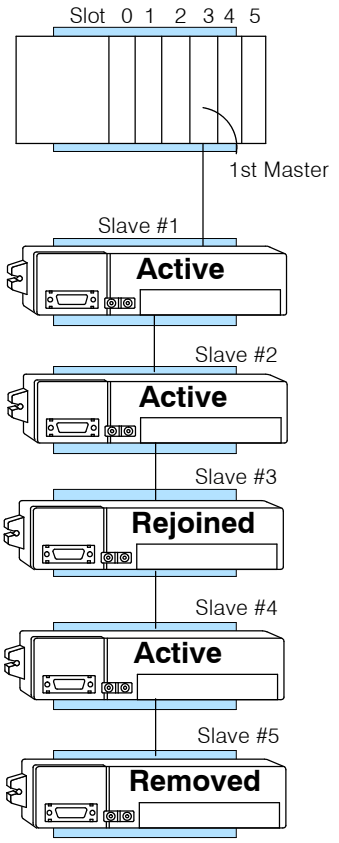
After power up, anytime a remote I/O error occurs for the 2nd Master, the input status will be frozen for the slave that has caused the error.

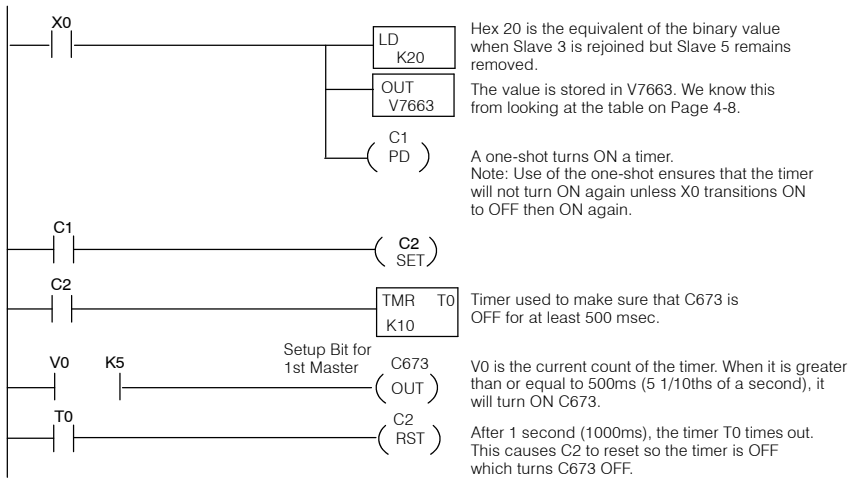
C673/C677 Activate Removal or Rejoining of Slaves

C673 is assigned to the 1st Master, and C677 to the 2nd. These relays have to be transitioned from OFF to ON in order to activate a setup written for removal and rejoining of slaves. They must be OFF for at least 500ms and ON for at least 500ms in order for the transition to be effective. In the example below, we are rejoining Slave 3 but Slave 5 remains removed. In this example, we are showing the 1st Master in slot 3 and I/O assignments had been made previously using manual addressing (ladder logic not shown here).

Example:

The diagram below shows the status after program execution.





V7663 (Status before the above is executed)

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0
Slave No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

V7663 (Status after the above is executed by transitioning C673)

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
Slave No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

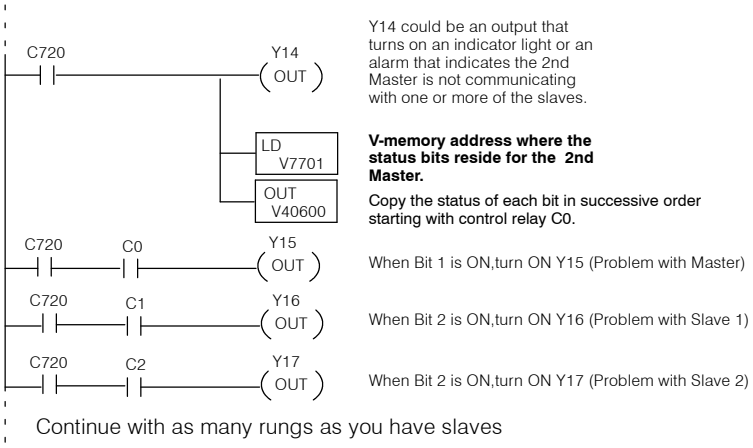
Note: Zero's in any of the bit positions mean that you want a slave to remain active if it is active or you want the slave rejoined if inactive. One's in any of the bit positions means that you want a slave to be removed if it is active or you want a slave to remain removed if already removed.

C700/C720 Locate Communications Error

These relays will be set when there is a **communications error** between the respective master and a slave or slaves assigned to the relay number. C700 is for the 1st Master and C720 is for the 2nd Master. In addition to these control relays, there are also V-memory locations that can be used to help pinpoint the error. V7700 is assigned to the 1st Master and V7701 is assigned to the 2nd Master.To specifically identify whether the problem is with the master or with one of its slaves, you can have your logic check specific bits in the corresponding V-memory.

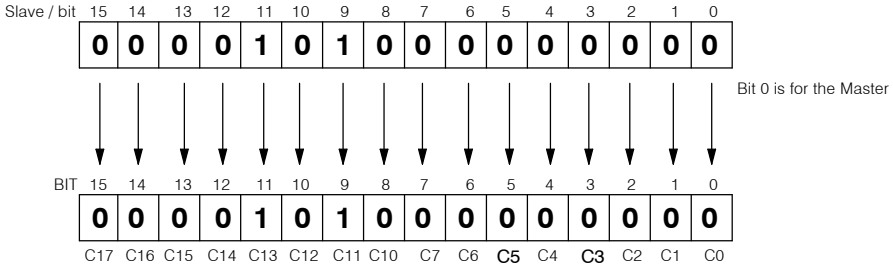
One easy way to do this is to load the contents of the V-memory location into the accumulator and then copy it to one of the V-memory locations that is assigned to control relays that are available for general use. Then, you can use these individual control relays inside of your ladder logic program to help pinpoint the error. In the following example, we used the charts in Appendix B to determine the V-memory address for C0-C17 (V40600). We loaded V7701, which is the communication error location for the 2nd Master, and then copied it to V40600.

Example:



Bit 0 is used to indicate a problem with the master, so the first control relay that contains slave information is C1. Also, notice how the control relays do not match up with the slave number after bit 7. This is because the control relays are numbered in octal, not decimal. For example, you'll notice that slave 9 is represented by C11.

V7701 - 2nd master with communication errors at Slaves 11 and 9



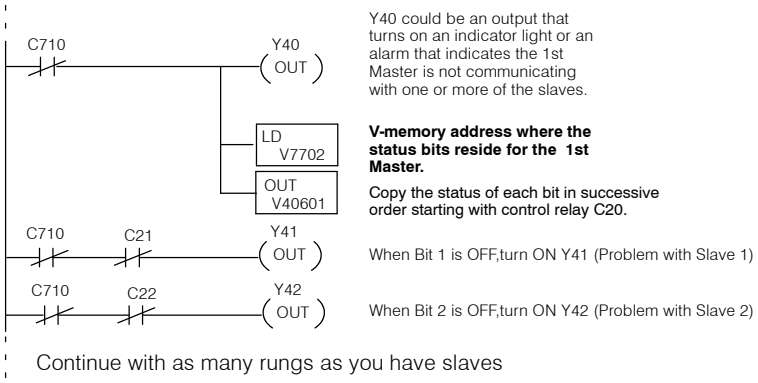
V40600 - Control Relays C0-C17

C710 and C730 Mapping O.K.

C710 is assigned to the 1st Master. C730 is assigned to the 2nd Master. If set, these flags indicate that the I/O points have been properly mapped. If they are off, then it indicates that a setup problem exists. In addition to these control relays, there are also V-memory locations that can be used to help pinpoint the error. V7702 is assigned to the 1st Master and V7703 is assigned to the 2nd Master. To specifically identify the location of the setup error, you can have your logic check specific bits in the corresponding V-memory.

One easy way to do this is to load the contents of the V-memory location into the accumulator and then copy it to one of the V-memory locations that is assigned to control relays that are available for general use. Then, you can use these individual control relays inside of your ladder logic program to help pinpoint the error. In the following example, we used the charts in Appendix B to determine the V-memory address for C20-C37 (V40601). We loaded V7702, which is the communication error location for the 1st Master, and then copied it to V40601.

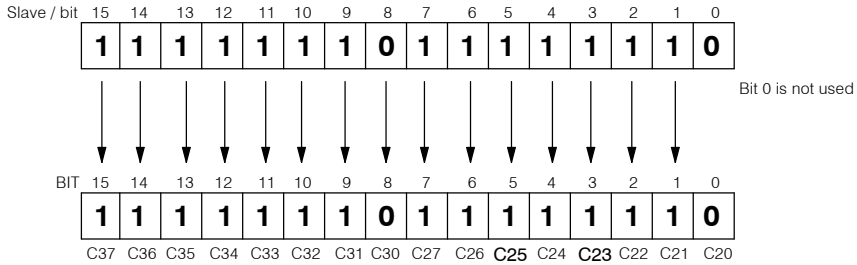
Example:



Note: C20 is not used here because the first bit does not mean anything for the mapping check.

Since bit 0 is not used, the first control relay that contains slave information is C21. Also, notice how the control relays relate to the slave number. You should remember that control relays are numbered in octal, not decimal. For example, you'll notice that slave 8 is represented by C30 in this example.

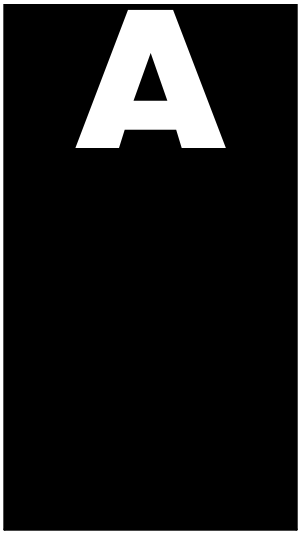
V7702 - 1st master showing that everything is O.K. except Slave 8 has not been mapped properly. (Remember, the bit is off when a problem exists.)



V40601 - Control Relays C20-C37

The only addressing mode that allows mapping of each individual slave is discrete addressing. This is how individual slaves can be mapped improperly and result in the error bit status shown above.

Appendix A
Slice I/O Worksheet



Master Module No. _____ Slave No. _____

Slice Slave Worksheet

Unit Address	Model Name	INPUT		OUTPUT	
		Input Address	No. Inputs	Output Address	No.Outputs
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					

Input Bit Start Address:_____ V-Memory Address:V_____

Total Input Points Consumed_____ Input Points Used_____

Output Bit Start Address:_____V-Memory Address:V_____

Total Output Points Consumed_____ Output Points Used_____

Appendix B
Memory Tables

B

— Standard Input (X) Addresses
— Standard Output (Y) Addresses
— Control Relay (C) Addresses
— Remote Input/Output Global (GX) Addresses

Standard Input (X) Addresses

MSB								LSB								Address
17	16	15	14	13	12	11	10	7	6	5	4	3	2	1	0	
017	016	015	014	013	012	011	010	007	006	005	004	003	002	001	000	V40400
037	036	035	034	033	032	031	030	027	026	025	024	023	022	021	020	V40401
057	056	055	054	053	052	051	050	047	046	045	044	043	042	041	040	V40402
077	076	075	074	073	072	071	070	067	066	065	064	063	062	061	060	V40403
117	116	115	114	113	112	111	110	107	106	105	104	103	102	101	100	V40404
137	136	135	134	133	132	131	130	127	126	125	124	123	122	121	120	V40405
157	156	155	154	153	152	151	150	147	146	145	144	143	142	141	140	V40406
177	176	175	174	173	172	171	170	167	166	165	164	163	162	161	160	V40407
217	216	215	214	213	212	211	210	207	206	205	204	203	202	201	200	V40410
237	236	235	234	233	232	231	230	227	226	225	224	223	222	221	220	V40411
257	256	255	254	253	252	251	250	247	246	245	244	243	242	241	240	V40412
277	276	275	274	273	272	271	270	267	266	265	264	263	262	261	260	V40413
317	316	315	314	313	312	311	310	307	306	305	304	303	302	301	300	V40414
337	336	335	334	333	332	331	330	327	326	325	324	323	322	321	320	V40415
357	356	355	354	353	352	351	350	347	346	345	344	343	342	341	340	V40416
377	376	375	374	373	372	371	370	367	366	365	364	363	362	361	360	V40417
417	416	415	414	413	412	411	410	407	406	405	404	403	402	401	400	V40420
437	436	435	434	433	432	431	430	427	426	425	424	423	422	421	420	V40421
457	456	455	454	453	452	451	450	447	446	445	444	443	442	441	440	V40422
477	476	475	474	473	472	471	470	467	466	465	464	463	462	461	460	V40423

Standard Output (Y) Addresses

MSB								LSB								Address
17	16	15	14	13	12	11	10	7	6	5	4	3	2	1	0	
017	016	015	014	013	012	011	010	007	006	005	004	003	002	001	000	V40500
037	036	035	034	033	032	031	030	027	026	025	024	023	022	021	020	V40501
057	056	055	054	053	052	051	050	047	046	045	044	043	042	041	040	V40502
077	076	075	074	073	072	071	070	067	066	065	064	063	062	061	060	V40503
117	116	115	114	113	112	111	110	107	106	105	104	103	102	101	100	V40504
137	136	135	134	133	132	131	130	127	126	125	124	123	122	121	120	V40505
157	156	155	154	153	152	151	150	147	146	145	144	143	142	141	140	V40506
177	176	175	174	173	172	171	170	167	166	165	164	163	162	161	160	V40507
217	216	215	214	213	212	211	210	207	206	205	204	203	202	201	200	V40510
237	236	235	234	233	232	231	230	227	226	225	224	223	222	221	220	V40511
257	256	255	254	253	252	251	250	247	246	245	244	243	242	241	240	V40512
277	276	275	274	273	272	271	270	267	266	265	264	263	262	261	260	V40513
317	316	315	314	313	312	311	310	307	306	305	304	303	302	301	300	V40514
337	336	335	334	333	332	331	330	327	326	325	324	323	322	321	320	V40515
357	356	355	354	353	352	351	350	347	346	345	344	343	342	341	340	V40516
377	376	375	374	373	372	371	370	367	366	365	364	363	362	361	360	V40517
417	416	415	414	413	412	411	410	407	406	405	404	403	402	401	400	V40520
437	436	435	434	433	432	431	430	427	426	425	424	423	422	421	420	V40521
457	456	455	454	453	452	451	450	447	446	445	444	443	442	441	440	V40522
477	476	475	474	473	472	471	470	467	466	465	464	463	462	461	460	V40523

Control Relay (C) Addresses

MSB								LSB								Address
17	16	15	14	13	12	11	10	7	6	5	4	3	2	1	0	
017	016	015	014	013	012	011	010	007	006	005	004	003	002	001	000	V40600
037	036	035	034	033	032	031	030	027	026	025	024	023	022	021	020	V40601
057	056	055	054	053	052	051	050	047	046	045	044	043	042	041	040	V40602
077	076	075	074	073	072	071	070	067	066	065	064	063	062	061	060	V40603
117	116	115	114	113	112	111	110	107	106	105	104	103	102	101	100	V40604
137	136	135	134	133	132	131	130	127	126	125	124	123	122	121	120	V40605
157	156	155	154	153	152	151	150	147	146	145	144	143	142	141	140	V40606
177	176	175	174	173	172	171	170	167	166	165	164	163	162	161	160	V40607
217	216	215	214	213	212	211	210	207	206	205	204	203	202	201	200	V40610
237	236	235	234	233	232	231	230	227	226	225	224	223	222	221	220	V40611
257	256	255	254	253	252	251	250	247	246	245	244	243	242	241	240	V40612
277	276	275	274	273	272	271	270	267	266	265	264	263	262	261	260	V40613
317	316	315	314	313	312	311	310	307	306	305	304	303	302	301	300	V40614
337	336	335	334	333	332	331	330	327	326	325	324	323	322	321	320	V40615
357	356	355	354	353	352	351	350	347	346	345	344	343	342	341	340	V40616
377	376	375	374	373	372	371	370	367	366	365	364	363	362	361	360	V40617
417	416	415	414	413	412	411	410	407	406	405	404	403	402	401	400	V40620
437	436	435	434	433	432	431	430	427	426	425	424	423	422	421	420	V40621
457	456	455	454	453	452	451	450	447	446	445	444	443	442	441	440	V40622
477	476	475	474	473	472	471	470	467	466	465	464	463	462	461	460	V40623
517	516	515	514	513	512	511	510	507	506	505	504	503	502	501	500	V40624
537	536	535	534	533	532	531	530	527	526	525	524	523	522	521	520	V40625
557	556	555	554	553	552	551	550	547	546	545	544	543	542	541	540	V40626
577	576	575	574	573	572	571	570	567	566	565	564	563	562	561	560	V40627
617	616	615	614	613	612	611	610	607	606	605	604	603	602	601	600	V40630
637	636	635	634	633	632	631	630	627	626	625	624	623	622	621	620	V40631
657	656	655	654	653	652	651	650	647	646	645	644	643	642	641	640	V40632
677	76	675	674	673	672	671	670	667	666	665	664	663	662	661	660	V40633
717	716	715	714	713	712	711	710	707	706	705	704	703	702	701	700	V40634
737	736	735	734	733	732	731	730	727	727	742	724	723	722	721	720	V40635

This portion of the table shows additional Control Relays points available with the DL440.

MSB								DL440 Additional Control Relays (C)							LSB	Address
17	16	15	14	13	12	11	10	7	6	5	4	3	2	1	0	
757	756	755	754	753	752	751	750	747	746	745	744	743	742	741	740	V40636
777	776	775	774	773	772	771	770	767	766	765	764	763	762	761	760	V40637
1017	1016	1015	1014	1013	1012	1011	1010	1007	1006	1005	1004	1003	1002	1001	1000	V40640
1037	1036	1035	1034	1033	1032	1031	1030	1027	1026	1025	1024	1023	1022	1021	1020	V40641
1057	1056	1055	1054	1053	1052	1051	1050	1047	1046	1045	1044	1043	1042	1041	1040	V40642
1077	1076	1075	1074	1073	1072	1071	1070	1067	1066	1065	1064	1063	1062	1061	1060	V40643
1117	1116	1115	1114	1113	1112	1111	1110	1107	1106	1105	1104	1103	1102	1101	1100	V40644
1137	1136	1135	1134	1133	1132	1131	1130	1127	1126	1125	1124	1123	1122	1121	1120	V40645
1157	1156	1155	1154	1153	1152	1151	1150	1147	1146	1145	1144	1143	1142	1141	1140	V40646
1177	1176	1175	1174	1173	1172	1171	1170	1167	1166	1165	1164	1163	1162	1161	1160	V40647
1217	1216	1215	1214	1213	1212	1211	1210	1207	1206	1205	1204	1203	1202	1201	1200	V40650
1237	1236	1235	1234	1233	1232	1231	1230	1227	1226	1225	1224	1223	1222	1221	1220	V40651
1257	1256	1255	1254	1253	1252	1251	1250	1247	1246	1245	1244	1243	1242	1241	1240	V40652
1277	1276	1275	1274	1273	1272	1271	1270	1267	1266	1265	1264	1263	1262	1261	1260	V40653
1317	1316	1315	1314	1313	1312	1311	1310	1307	1306	1305	1304	1303	1302	1301	1300	V40654
1337	1336	1335	1334	1333	1332	1331	1330	1327	1326	1325	1324	1323	1322	1321	1320	V40655
1357	1356	1355	1354	1353	1352	1351	1350	1347	1346	1345	1344	1343	1342	1341	1340	V40656
1377	1376	1375	1374	1373	1372	1371	1370	1367	1366	1365	1364	1363	1362	1361	1360	V40657
1417	1416	1415	1414	1413	1412	1411	1410	1407	1406	1405	1404	1403	1402	1401	1400	V40660
1437	1436	1435	1434	1433	1432	1431	1430	1427	1426	1425	1424	1423	1422	1421	1420	V40661
1457	1456	1455	1454	1453	1452	1451	1450	1447	1446	1445	1444	1443	1442	1441	1440	V40662
1477	1476	1475	1474	1473	1472	1471	1470	1467	1466	1465	1464	1463	1462	1461	1460	V40663
1517	1516	1515	1514	1513	1512	1511	1510	1507	1506	1505	1504	1503	1502	1501	1500	V40664
1537	1536	1535	1534	1533	1532	1531	1530	1527	1526	1525	1524	1523	1522	1521	1520	V40665
1557	1556	1555	1554	1553	1552	1551	1550	1547	1546	1545	1544	1543	1542	1541	1540	V40666
1577	1576	1575	1574	1573	1572	1571	1570	1567	1566	1565	1564	1563	1562	1561	1560	V40667
1617	1616	1615	1614	1613	1612	1611	1610	1607	1606	1605	1604	1603	1602	1601	1600	V40670
1637	1636	1635	1634	1633	1632	1631	1630	1627	1626	1625	1624	1623	1622	1621	1620	V40671
1657	1656	1655	1654	1653	1652	1651	1650	1647	1646	1645	1644	1643	1642	1641	1640	V40672
1677	1676	1675	1674	1673	1672	1671	1670	1667	1666	1665	1664	1663	1662	1661	1660	V40673
1717	1716	1715	1714	1713	1712	1711	1710	1707	1706	1705	1704	1703	1702	1701	1700	V40674
1737	1736	1735	1734	1733	1732	1731	1730	1727	1726	1725	1724	1723	1722	1721	1720	V40675
1757	1756	1755	1754	1753	1752	1751	1750	1747	1746	1745	1744	1743	1742	1741	1740	V40676
1777	1776	1775	1774	1773	1772	1771	1770	1767	1766	1765	1764	1763	1762	1761	1760	V40677

Remote Input/Output Global (GX) Addresses

MSB								LSB								Address
17	16	15	14	13	12	11	10	7	6	5	4	3	2	1	0	
017	016	015	014	013	012	011	010	007	006	005	004	003	002	001	000	V40000
037	036	035	034	033	032	031	030	027	026	025	024	023	022	021	020	V40001
057	056	055	054	053	052	051	050	047	046	045	044	043	042	041	040	V40002
077	076	075	074	073	072	071	070	067	066	065	064	063	062	061	060	V40003
117	116	115	114	113	112	111	110	107	106	105	104	103	102	101	100	V40004
137	136	135	134	133	132	131	130	127	126	125	124	123	122	121	120	V40005
157	156	155	154	153	152	151	150	147	146	145	144	143	142	141	140	V40006
177	176	175	174	173	172	171	170	167	166	165	164	163	162	161	160	V40007
217	216	215	214	213	212	211	210	207	206	205	204	203	202	201	200	V40010
237	236	235	234	233	232	231	230	227	226	225	224	223	222	221	220	V40011
257	256	255	254	253	252	251	250	247	246	245	244	243	242	241	240	V40012
277	276	275	274	273	272	271	270	267	266	265	264	263	262	261	260	V40013
317	316	315	314	313	312	311	310	307	306	305	304	303	302	301	300	V40014
337	336	335	334	333	332	331	330	327	326	325	324	323	322	321	320	V40015
357	356	355	354	353	352	351	350	347	346	345	344	343	342	341	340	V40016
377	376	375	374	373	372	371	370	367	366	365	364	363	362	361	360	V40017
417	416	415	414	413	412	411	410	407	406	405	404	403	402	401	400	V40020
437	436	435	434	433	432	431	430	427	426	425	424	423	422	421	420	V40021
457	456	455	454	453	452	451	450	447	446	445	444	443	442	441	440	V40022
477	476	475	474	473	472	471	470	467	466	465	464	463	462	461	460	V40023
517	516	515	514	513	512	511	510	507	506	505	504	503	502	501	500	V40024
537	536	535	534	533	532	531	530	527	526	525	524	523	522	521	520	V40025
557	556	555	554	553	552	551	550	547	546	545	544	543	542	541	540	V40026
577	576	575	574	573	572	571	570	567	566	565	564	563	562	561	560	V40027
617	616	615	614	613	612	611	610	607	606	605	604	603	602	601	600	V40030
637	636	635	634	633	632	631	630	627	626	625	624	623	622	621	620	V40031
657	656	655	654	653	652	651	650	647	646	645	644	643	642	641	640	V40032
677	76	675	674	673	672	671	670	667	666	665	664	663	662	661	660	V40033
717	716	715	714	713	712	711	710	707	706	705	704	703	702	701	700	V40034
737	736	735	734	733	732	731	730	727	727	742	724	723	722	721	720	V40035
757	756	755	754	753	752	751	750	747	746	745	744	743	742	741	740	V40036
777	776	775	774	773	772	771	770	767	766	765	764	763	762	761	760	V40037

C

Appendix C Determining I/O Update Time

— Overview
— Calculating Input Signal Delay Time
— Calculating Output Signal Delay Time
— Calculating Total System Delay Time

Overview

Since the Slice Master and the CPU operate asynchronously from one another, it is possible that the remote I/O points may not be updated on every CPU scan. Therefore, if you have I/O points that must be updated on every scan, you should place them in the local and/or expansion base. In some applications it may helpful to understand the amount of time required to update the Slice I/O points. Depending on the number of I/O points used in your Slice configuration and the baud rate you have selected for communication, your update time requirements will vary. This Appendix will show you how to estimate the total delay time for your system.

NOTE: In most situations, this delay will be so small that either it makes no difference to the particular application or the mechanical speeds of the field devices are slower than the delay itself.

If you have an application that requires a thorough understanding of the time delay, you can use the following information in order to calculate the delay:

- **Baud Rate —** this is the communication baud rate that you selected with the dipswitch settings on the slice master and slice slaves.
- **CPU Scan Time —** this is the total CPU scan time. The easiest way is to use AUX53 from a DL405 Handheld Programmer, or use the Diagnostics option under the PLC menu in our ***Direct***SOFT Programming Software. You can also use the DL405 User Manual to calculate the scan time, but this is often very time consuming. If you use the User Manual, you will have to estimate this time, because it is dependent on the main program length, and number of I/O points in the local and expansion bases as well.
- **Slice Master Scan —** this is the time required for the Slice Master to scan the individual Slave stations to update the status of the I/O modules. Use the formula and table shown on the following page.
- **Module ON to OFF, OFF to ON Response Time —** this is the amount of time that the module requires to see a transition in status. For example, when a switch connected to an input module closes, it can take a few milliseconds (1–12 typical) before the module actually makes the transition from OFF to ON. Check the detailed specifications in Chapter 1 for the Slice slave response times. This basic information is also available in the specifications of the Sales Catalog.
- **Total Delay Time —** this is the total delay time that takes all of the above factors into consideration. There are several formulas that can be used to calculate this delay time. The pages that follow will show you those formulas. Once you have selected the applicable formula, you will use the information you have gathered for the above items to calculate the total system delay time.

Since each application is different, we cannot possibly show all of the options for the CPU scan time or the possible module response delays. You can easily find this information in other publications. However, the next few pages *will* show you how to calculate the delay time for the Slice Master Scan. Also, we show the total delay time for our example system that was used earlier in this manual.

Calculating Input Signal Delay Time

Input Delay Time Formulas

The formulas shown below show you how much time is required for the CPU to detect an OFF-to-ON transition for an input switch at the slave station.

- Minimum Delay: I_{min} = F+910 μs
- Maximum Delay: I_{max} = F+2B +C

F = Time delay for input filter(s)
ON to OFF = 12 ms (maximum)
OFF to ON = 7 ms (maximum)
B = Bus scan time (See table below.)
C = CPU scan time (With ***Direct***SOFT, click on PLC/Diagnostics/Scan Time)
As an alternative, use AUX53 of the handheld programmer to find this out.

Slot Location of the Master	V-memory Location where the bus scan time is calculated and stored as a hexadecimal number of milliseconds
0	V7710
1	V7711
2	V7712
3	V7713
4	V7714
5	V7715
6	V7716
7	V7717

Example for Computing Input Delay

In this example, we are examining the OFF to ON transition for the input delay of a slave belonging to a master that is located in Slot 2 of the CPU base.

1. Use the maximum delay formula: I_{max} = F+2B +C
2. Use 7ms maximum filter delay time.
3. Place the CPU in RUN mode.
4. Use the table above to find the memory location that contains the bus scan time. For example, let's say it is 12ms.
5. Use ***Direct***SOFT or AUX 53 from a handheld programmer to determine the CPU scan time. For illustration, let's say you discover it is 20 ms.
6. Solve the equation from Step 1:
   I_{max} = F + 2B +C
   I_{max} = 7 + 2(12) +20
   I_{max} = 51ms

Calculating Output Signal Delay Time

Output Delay Time Formulas

Here we are measuring the amount of time it takes for the CPU to turn ON an output at the Slice Slave. The formulas for computing this are as follows:

- OUT_{min} = 1.12 ms
- OUT_{max} = 0.5 ms + 2B +C

OUT_{min} = Minimum output signal delay
OUT_{max} =Maximum output signal delay
0.5 ms = Output hardware response time
B =Bus scan time (See Table Below.)
C = CPU scan time (follow instructions on Page C-3)

Slot Location of the Master	V-memory Location where the bus scan time is calculated and stored as a hexadecimal number of milliseconds
0	V7710
1	V7711
2	V7712
3	V7713
4	V7714
5	V7715
6	V7716
7	V7717

Example for Computing Output Delay

In this example, we are examining the maximum time an output point is delayed when transitioning from OFF to ON. Here we are measuring an output point on a slave belonging to a master located in Slot 4.

1. Use the maximum delay formula: OUT_{max} = 0.5ms + 2B +C
2. Place the CPU in the RUN mode.
3. Use the table to find where to check in memory for the bus scan time. For illustration, let's say you discover it is 15 ms.
4. Use ***Direct***SOFT or AUX53 of the handheld programmer to determine the CPU scan time. For illustration, let's say you discover it is 12 ms.
5. Solve the equation from Step 1:
   OUT_{max} = 0.5 ms + 2B + C
   OUT_{max} = 0.5 ms + 2(15) + 12
   OUT_{max} = 42.5 ms

Calculating Total System Delay Time

Output Delay Time Formulas

Here we are calculating the total delay time for a simple Slice I/O example. Once the Slice slave input comes on, we want to know how long it will take the system to sense the input change, transfer the data back to the CPU, and then update the Slice slave output point.The formulas for computing this are as follows:

- $TOT_{min} = I_{min} + B + C$
- $TOT_{max} = I_{max} + 4B + C$
- $TOT_{avg} = I_{min} + 2B + C$

TOT_{min} = Minimum total signal delay
TOT_{max} = Maximum total signal delay
TOT_{avg} = Average total signal delay
I_{max} = Maximum input signal delay
I_{min} = Minimum input signal delay
B =Bus scan time (See Table Below.)
C = CPU scan time (follow instructions on Page C-3)

Slot Location of the Master	V-memory Location where the bus scan time is calculated and stored as a hexadecimal number of milliseconds
0	V7710
1	V7711
2	V7712
3	V7713
4	V7714
5	V7715
6	V7716
7	V7717

Table Showing Approximate Signal Delay Times

Before you actually do your own computations using the formulas above, you may want to have an approximate idea of how much total delay time you should expect. This table should provide that information. We leave the actual computation up to you. In this example, we are assuming that we are using a 440 CPU and the scan time for a hypothetical example program is 20 ms (Use ***Direct***SOFT or AUX53 to find the time for your program). We are also assuming a baud rate of153.6 kB between the Slice Master and the Slice Slaves.

# of Remotes	TOTmin (ms)	TOTavg (ms)	Tmax (ms)
2	30.7	34.3	41.6
4	34.2	41.4	55.8
6	37.8	48.5	70.0
8	41.3	55.6	84.2
10	44.8	62.7	92.7
12	48.4	69.7	112.4