Tables

B

In This Appendix. . . .

— DeviceNet Tables

Data Input and Output Tables

Input Register Object Class (107)

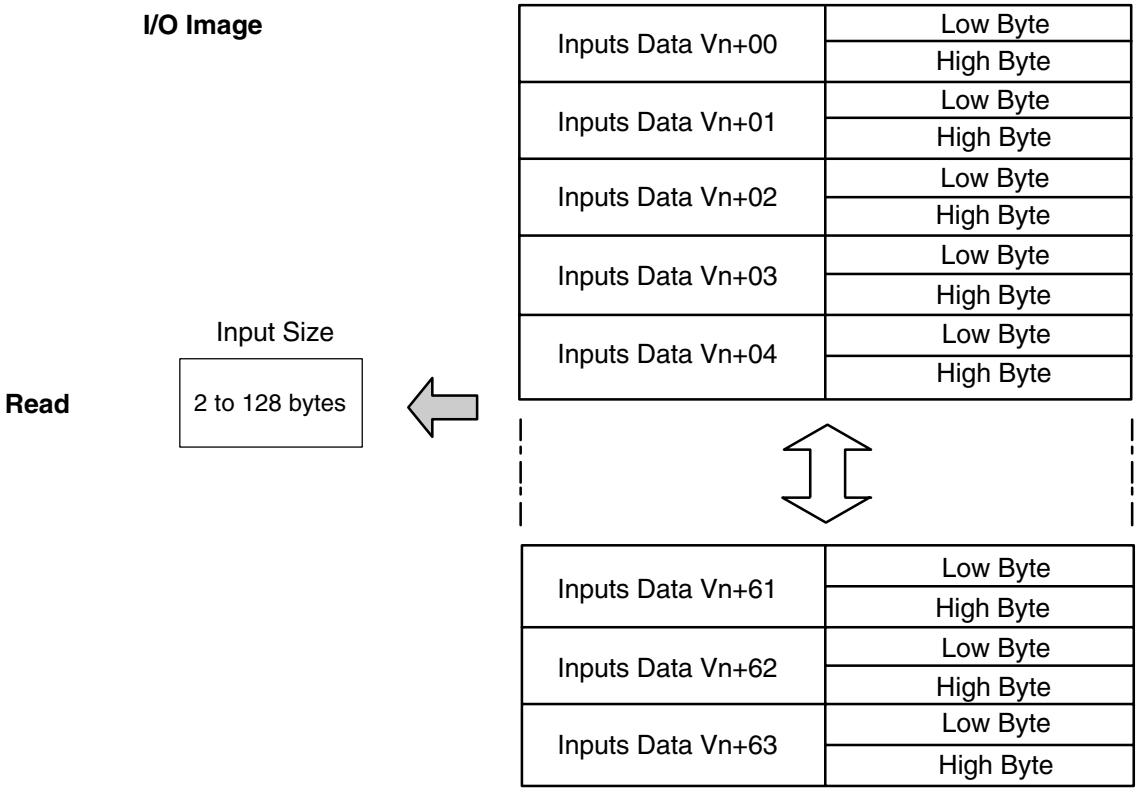
Instance = 1 Attribute = 3

Name	Data	Address	Service
Input Register	Vn+00	+00	Get
	Vn+01	+02	
	Vn+02	+04	
	Vn+03	+06	
	Vn+04	+08	
	:	:	
	Vn+62	+124	
	Vn+63	+ 126	

The Data Register equals one Word (16 bits).
A maximum of 64 V–memory words can be accessed.

Input Register

Register Input (V–memory) Image Table Mapping



Bit	07	06	05	04	03	02	01	00	Size
	Vn + 00 V memory Low byte data								Read Byte 1
	Vn + 00 V memory High byte data								Read Byte 2
	Vn + 01 V memory Low byte data								Read Byte 3
	Vn + 01 V memory High byte data								Read Byte 4
	Vn + 02 V memory Low byte data								Read Byte 5
	Vn + 02 V memory High byte data								Read Byte 6
	:								:
	:								:
	Vn + 60 V memory Low byte data								Read Byte 121
	Vn + 60 V memory High byte data								Read Byte 122
	Vn + 61 V memory Low byte data								Read Byte 123
	Vn + 61 V memory High byte data								Read Byte 124
	Vn + 62 V memory Low byte data								Read Byte 125
	Vn + 62 V memory High byte data								Read Byte 126
	Vn + 63 V memory Low byte data								Read Byte 127
	Vn + 63 V memory High byte data								Read Byte 128

Output Register Object Class (108)

Instance = 1 Attribute = 3

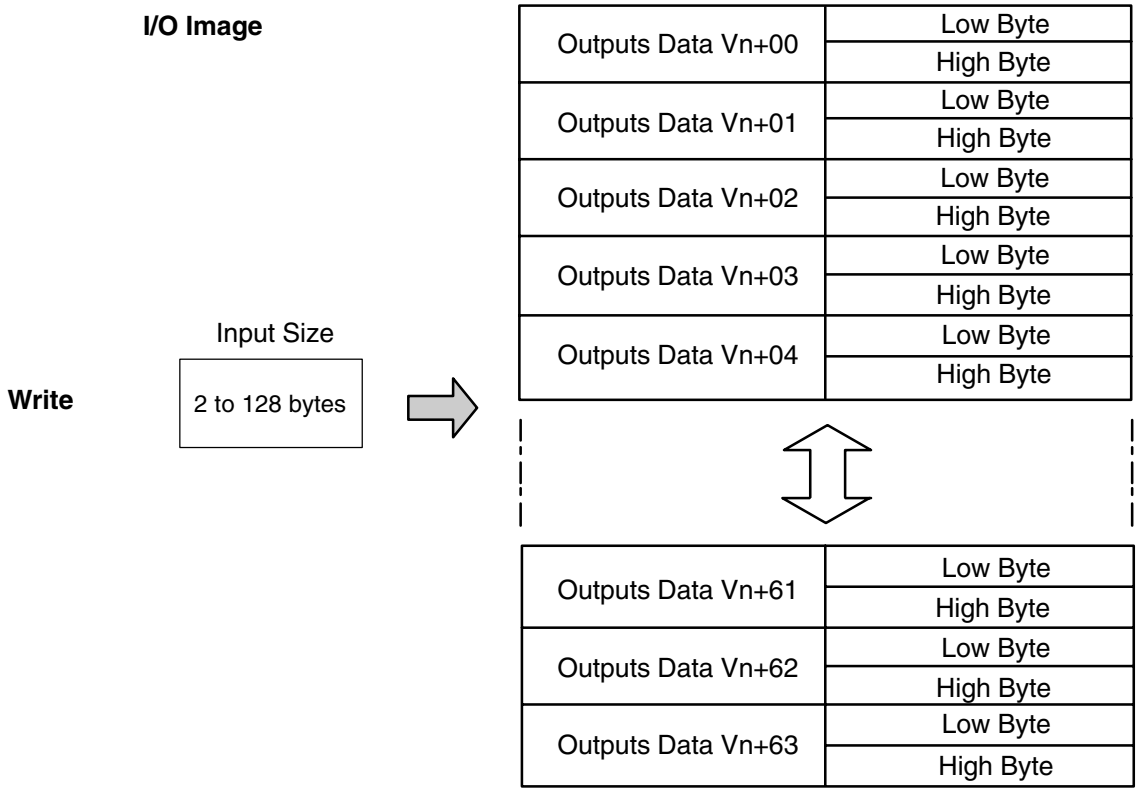
Name	Data	Address	Service
Output Register	Vn+00	+00	Set
	Vn+01	+02	
	Vn+02	+04	
	Vn+03	+06	
	Vn+04	+08	
	:	:	
	Vn+62	+124	
	Vn+63	+ 126	

The Data Register equals one Word (16 bits).

A maximum of 64 V–memory words can be accessed.

Output Register

Register Output (V–memory) Image Table Mapping



Bit	07	06	05	04	03	02	01	00	Size
	Vn + 00 V memory Low byte data								Write Byte 1
	Vn + 00 V memory High byte data								Write Byte 2
	Vn + 01 V memory Low byte data								Write Byte 3
	Vn + 01 V memory High byte data								Write Byte 4
	Vn + 02 V memory Low byte data								Write Byte 5
	Vn + 02 V memory High byte data								Write Byte 6
	:								:
	:								:
	Vn + 60 V memory Low byte data								Write Byte 121
	Vn + 60 V memory High byte data								Write Byte 122
	Vn + 61 V memory Low byte data								Write Byte 123
	Vn + 61 V memory High byte data								Write Byte 124
	Vn + 62 V memory Low byte data								Write Byte 125
	Vn + 62 V memory High byte data								Write Byte 126
	Vn + 63 V memory Low byte data								Write Byte 127
	Vn + 63 V memory High byte data								Write Byte 128

Data Register Range

RJ12 serial port supports the following registers.

No.	Register Number	Comment	Description
1	V40400–V40477	Input Register	Read/Write
2	V40500–V40577	Output Register	Read/Write
3	V00000–V02777	Data Register	Read/Write
4	V03000–V03077	Explicit Get Command Area	Read/Write
5	V03100–V03177	Explicit Set Command Area	Read/Write
6	V03200–V07377	Data Register	Read/Write
7	V07640–V07613	Special Register	Resave
8	V07614–V07617	Parameter Register	Read
9	V07620–V07777	Special Register	Resave

Note: Not all registers back up data.

I/O Diagnostic Information

DIP Switch SW4

The position of DIP Switch SW4 determines whether or not you receive Terminator I/O diagnostic information. If SW4 is in the OFF (default) position, you will receive this diagnostic information and you must allow for two additional bytes on the input (RX) and two additional bytes on the output (TX) for Terminator I/O diagnostic functions.

If SW4 is placed in the ON position, you will not receive this diagnostic information and there is no need to allow for the additional bytes.

Following is a description of the diagnostic codes.

Diagnostic (polling) information whenT1K–DEVNETS (slave) transmits to a master.

Address	Bytes	Data	Comment	
+0	1	I/O Status	Bit 0: Missing module error ON: Error / OFF: Normal	
			Bit 1: New module present error ON: Error / OFF: Normal	
			Bit 2: I/O diagnostic error ON: Error / OFF: Normal	
			Bit 3: Node error (the node number has changed) ON: Error / OFF: Normal	
			Bit 4: Idle (Output is idle) ON: Idle / OFF: Normal	
			Bit 5: Multiple error (Two or more errors occurred) ON: Multiple / OFF: Normal	
			Bit 7: Output status ON: Enable / OFF: Disable	
+1	1	Error Slot	01h: Slot 1 02h: Slot 2 . . 1Fh: Slot 31	Module Missing error or New Module Error
			21h: Slot 1 22h: Slot 2 . . 3Fh: Slot 31	24V Error or Fuse Error
			The slot number in which the error has occurred. When the same error occurs by multiple slots, priority is given to low slot number. Priority is given to 24V Error or Fuse Error when multiple errors occur at the same time.	
+2 . +nn	n	Bit Data	T1K–DEVNETS input module data.	

Diagnostic (polling) information when a master transmits to a T1K–DEVNETS (slave). The command to select I/O configuration is transferred from peripheral and written here. When the I/O configuration error occurs the command is executed.

Address	Bytes	Data	Comment
+0	1	Code of except the following	No request
		5Ah	Select I/O reconfiguration
		C3h	Select Output Enable
		3Ch	Select Output Disable
+1	1	Reserved	Not used
+2 . +nn	n	Bit data	T1K–DEVNETS output module data.

System Information Object Specifications

DeviceNet object that T1K–DEVNETS supports are:

Item		Instance	Class Number
Special Object	System Information Object	1–4	106