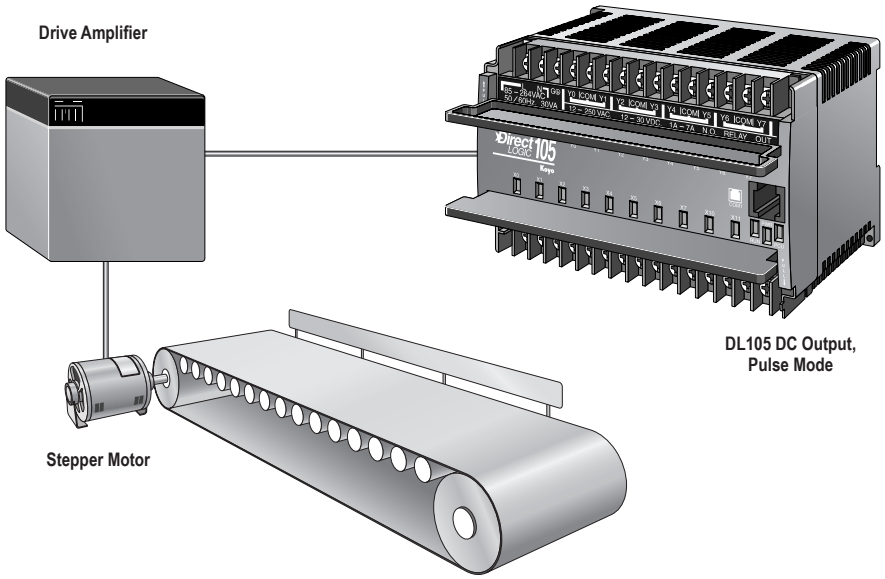
Built-in High-Speed I/O Features

Selected DL105 micro PLCs offer special high-speed input features (on units with DC inputs) and pulse output features (on units with DC outputs). These features are available on the first four input points (X0–X3) and the first two output points (Y0–Y1). This allows you to use the economical DL105 micro PLC to solve a diverse range of high-speed machine control applications.

There are several modes of operation from which to choose. Here's a brief description of the modes provided.

- Single 5kHz high-speed counter with 24 presets. When the preset is reached, an interrupt routine is executed.
- Single quadrature encoder input (up/down counter) for clockwise and counterclockwise position control.
- Single-channel programmable 7kHz pulse output with an external interrupt and separate acceleration/deceleration profiles for positioning and velocity control.
- A single external interrupt input for an immediate response to time-critical tasks.
- Single pulse catch input allows the CPU to read an input with a pulse width as small as 0.1 ms.
- Four inputs with selectable filters (0-99 ms) to ensure input signal integrity. This is the default mode, which is set at 10ms filter.



- A single timed interrupt that can be scheduled on a 5ms – 999ms cycle. (All units have this feature.)

Combine features to use the full potential of the module. Some modes do not use all available points, so in some cases you can assign one of the other features to the point(s) not used by the main mode of operations.

You cannot use the DL105 for closed-loop control. You cannot use the Up counter and pulse output features at the same time.

You can easily select the mode of operation just by entering an appropriate "code" in a special CPU V-memory location. These features are explained in more detail later in this section. Remember, not all features can be used at the same time. The Counter Mode Options table provides point-by-point usage for each mode of operation.

Counter Mode Options

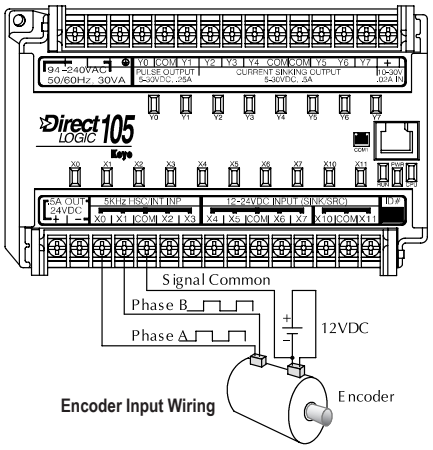
Mode	DC Input Points				DC Output Points	
	X0	X1	X2	X3	Y0	Y1
Filtered Input	Filtered Input	Filtered Input	Filtered Input	Filtered Input	Regular Output	Regular Output
Up Counter	Count Input	Filtered Input	Filtered Input, or Counter Reset	Filtered Input	Regular Output	Regular Output
Up/Down Counter	Phase A Input	Phase B Input	Filtered Input, or Counter Reset	Filtered Input	Regular Output	Regular Output
Interrupt Input	Interrupt Input	Filtered Input	Filtered Input	Filtered Input	Regular Output	Regular Output
Pulse Catch	Pulse Catch	Filtered Input	Filtered Input	Filtered Input	Regular Output	Regular Output
Pulse Output	Not available for use	Filtered Input	Filtered Input, or Interrupt to Trigger Pulse Output	Filtered Input	Pulse or CW Output	Direction or CCW Output
Timed Interrupt	Filtered Input	Filtered Input	Filtered Input	Filtered Input	Regular Output	Regular Output

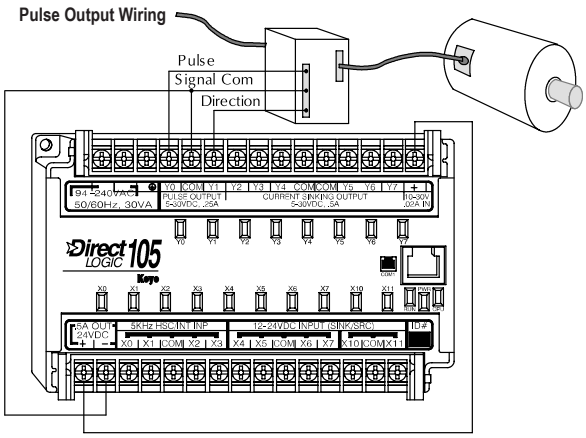
Built-in High-Speed I/O Specifications

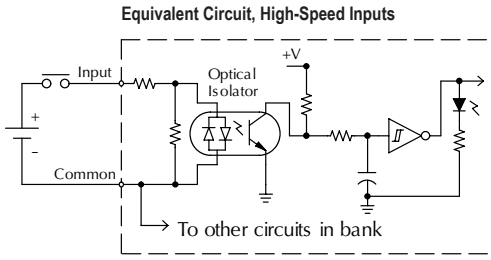
High-Speed Input Specifications	
Inputs	4 pts. max., X0-X3, sink or source 5kHz max.
Minimum Pulse Width	100µs
Input Voltage Range	10–26.4 VDC
Input Impedance	3.0 kq @ 12VDC 2.8 kq @ 24VDC
ON Current/Voltage Level	> 3mA / > 9VDC
OFF Current/Voltage Level	< 0.5 mA / < 2VDC
OFF to ON Response	< 50µs
ON to OFF Response	< 50µs

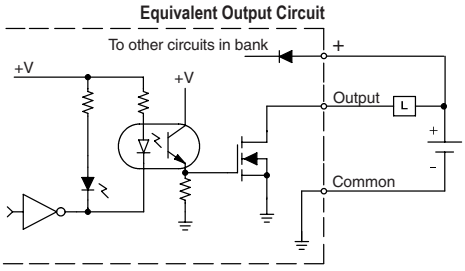
High-Speed Output Specifications	
Outputs	2 pts. Max., Y0&Y1 current sinking, 7kHz Max.
Voltage Range	5–30 VDC
Maximum Load Current	0.5 A/point
ON Voltage Drop	0.45 VDC @ 0.5 A
Leakage Current	15µA @ 30VDC
Inrush Current	1.5 A (10ms) 0.5 A (100ms)
OFF to ON Response	< 50µs
ON to OFF Response	< 50µs

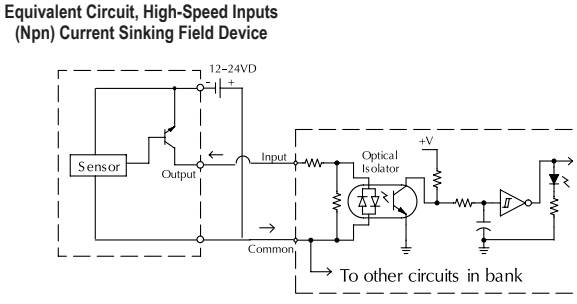
Wiring Diagrams

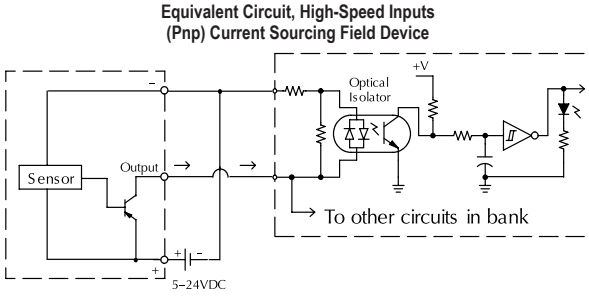












Understanding the Timed Interrupt

Overview

There is a timed interrupt feature available in the DL105 micro PLCs. This cyclical interrupt allows you to easily program a time-based interrupt that occurs on a scheduled basis. This feature is available in all units, regardless of input type.

The CPU's timed interrupt operates in a manner similar to the external interrupt input, but instead of the interrupt subroutine being triggered by an external event tied to X0, it is now triggered by a cyclical interval of time. This interval can be programmed from 5ms to 999ms. Whenever the programmed time elapses, the CPU immediately suspends its routine scan cycle and jumps to interrupt subroutine INT0.

When the subroutine execution is complete, the CPU automatically resumes its routine scan cycle starting from the exact location where it was interrupted. Since the CPU scan time and the interrupted time interval are different, the RLL program gets interrupted at various points in the execution over time. This does not present a problem. The CPU always returns to the point where it left to resume the program execution.

Input assignments for timed interrupt mode

X0:.....Filtered input (uses filter time set for X1)
X1:.....Filtered input
X2:.....Filtered input
X3:.....Filtered input

Timed interrupt specification

Timed interrupts.....1 (internal to CPU)
Time interval.....5 to 999 ms (1ms increments)
Interrupt subroutine.....NT0